DEVELOPMENT OF A POWER SILICON GATE CONTROLLED SWITCH

By Max P. Schreiner

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TABLE OF CONTENTS

Title	Page
ABSTRACT	vii
NARRATIVE AND DATA	1
1.00 THEORETICAL CONSIDERATIONS	1
2.00 DESIGN REQUIREMENTS	5
3.00 PROJECT PROGRAMS	7
3.10 LIFETIME CONTROL	7
3.20 GEOMETRY EFFECTS	10
3.30 DIFFUSION TECHNOLOGY	11
4.00 DEVICE FABRICATION	13
5.00 EVALUATION OF RESULTS AND TEST EQUIPMENT	14
CONCLUSIONS	16

LIST OF ILLUSTRATIONS

Figure	Title	Page
1	PNPN Transistor Analysis	17
2	PNPN Alpha Configuration	18
3	Anode E-I Characteristics	18
4	Quenching Apparatus	19
5	Parameter Distributions of Quenching Runs	20
6	Depletion Layer Impurity Distribution	21
7	E Pattern Configuration	22
8	Concentric Parallel-Gate Configuration	23
9	Cross Section of Concentric Ring-Gate Structure	24
10	Picture of Power Switching Material Damage	24
11	Cross Section of Concentric Parallel-Gate Structure	25
12	Typical Anode Saturation Characteristic	26
13	Three Terminal Frequency Characteristics	27
14	DC Alpha Characteristics (N24A)	28
15	DC Alpha Characteristics (N7A)	29
16	Typical Turn-Off Beta Characteristics	30
17	Gate Dynamic Switching Characteristics	31
18	Anode Voltage Switching Characteristics	32
19	Anode Current Switching Characteristics	33
20	$I_{gr}/I_{gt(off)}$ Switching Characteristics	34
21	10 Amp - G.C.S. Flow Chart	35
22	Alignment Pattern	36
23	N - Emitter Pattern	36
24	Nickel Plating Pattern	36
25	Cavitron Alignment Jig	37
26	Cavitroned Wafer	38
27	Soldered Cell	38

LIST OF ILLUSTRATIONS - (Contd.)

Figure	Title	Page
28	Package Outline	39
29	Completed Device	40
30	Power Switching Test Set	41
31	Schematic of Power Switching Test Set	42
32	Device Turn-On Time Characteristics	43
33	Device Turn-Off Time Characteristics	43
34	Dynamic Gate Switching Impedance	43
35	Schematic of B_{off} Test Set	44
36	Thermal Impedance Equipment	45
37	PNPN Curve Tracer Test Set	46
38	Schematic of PNPN Curve Tracer	47
39	Schematic of Anode Surge Test Set	48
40	Summary of Device Final Test Data	49

Abstract

This final report describes the development programs initiated to meet the device requirements of high voltage - high current switching at turn-off gains and power switching levels not obtainable from existing commercial devices. The theory of gate control switch design is discussed, and a summary of three project programs is given: (1) Life time control, (2) Geometry effects, (3) Diffusion technology. Device fabrication and evaluation techniques are described with the device experimental data and results. The conclusions of the development program based upon the results obtained complete the report.

AUTHOR

Theoretical Consideration

1.00 Silicon controlled rectifiers have experienced considerable improvement since their relatively recent beginning. Papers giving theoretical relationships of the four layer PNPN to the more familiar transistor have resulted in a fairly thorough understanding of the basic mechanisms of controlled rectifier operation. These devices have the characteristic common to the gas tube thyratron in their failure to be able to alter the anode current with the control element after the current has been initiated. Silicon controlled rectifiers with gate turn-off gain are therefore desirable, and devices capable of relatively low power applications are just becoming available commercially. Gate turn-off controlled rectifiers capable of high current operation turning off into a high voltage source are described in the report. These devices will be referred to as "Gate Controlled Switches" for the remainder of the report.

1.10 Figure 1 shows the PNPN four layer configuration for controlled rectifiers along with the equivalent two transistor structure. When a positive potential is applied to the P-emitter, or anode of the device, with respect to the N-emitter, or cathode of the device, junctions J_1 and J_3 are forward biased and the center P-base - N-base junction (J_2) is reversed biased.

Neglecting the surface leakage of the junction J_2, the saturation leakage of the device may be obtained by assuming currents in the two transistor equivalent and solving for the saturation leakage current. The total external forward current in terms of the saturation leakage and the individual transistor current gains (α_{NPN} and α_{PNP}) is given in Equation 1.11.

$$I_F = \frac{\alpha_{NPN} I_g + I_s}{1 - (M_N \alpha_{NPN} + M_P \alpha_{PNP})} \qquad 1.11$$

I_F = external forward device current

I_g = device gate current

I_s = saturation leakage current

M_N = multiplication factor associated with electrons

M_P = multiplication factor associated with holes

α_{NPN} = current gain associated with the NPN transistor

α_{PNP} = current gain associated with the PNP transistor

As the positive anode potential is increased, the device reaches a voltage where the multiplication factors become the determining quantities. J. L. Mole, M. Tanenbaum, J. M. Goldey and N. Holonyak (1) show that Equation 1.12 is an identity at the point of breakover.

$$M_N \ \alpha_{NPN} + M_P \ \alpha_{PNP} = 1 \qquad 1.12$$

Very little error is introduced in the analysis if the electron and hole multiplication factors are assumed equal.

$$M = \frac{1}{\alpha_{NPN} + \alpha_{PNP}} \qquad 1.13$$

The multiplication process is a function of applied voltage, but the relative number of minority carriers available for the multiplication process is a function of current. The relationship of the applied voltage to the avalanche characteristics of the device is given in Equation 1.14

$$\frac{V_f}{V_b} = (1 - \alpha_{NPN} - \alpha_{PNP})^{1/n} \qquad 1.14$$

V_f = positive device anode voltage

V_b = device breakover characteristics

n = constant equal to ≈ 2 to 3 for silicon

By substitution, Equation 1.15 shows the relationship of the multiplication factors to the applied voltage.

$$M = \frac{1}{1 - \left(\frac{V_f}{V_b}\right)^n} \qquad 1.15$$

When the device voltage (V_f) is zero, M approaches unity. When the device voltage increases to the device breakover value (V_b), M approaches infinity. The normal V_f of a device in the conducting state is small compared to the device breakover voltage (V_b) and therefore M is assumed to be unity. Since the saturation leakage (I_s) is insignificant compared to the device conduction current, Equation 1.11 reduces to Equation 1.16 during the device conduction interval.

$$I_f = \frac{\alpha_{NPN} I_g}{1 - (\alpha_{NPN} + \alpha_{PNP})} \qquad 1.16$$

$$B_{off} = \frac{I_f}{-I_g} \qquad 1.17$$

$$B_{off} = \frac{\alpha_{NPN}}{\alpha_{NPN} + \alpha_{PNP} - 1} \qquad 1.18$$

The gate turn-off gain (B_{off}) is defined in Equation 1.17 and Equation 1.18 gives an expression of the device turn-off gain in terms of the equivalent transistor current gains with the device in the conducting state. When the device voltage (V_f) increases, during the turn-off interval, to a value approaching the device breakover characteristic (V_b), Equation 1.18 will be altered by the increasing multiplication factors (M) affecting the ($M \alpha$) product terms of Equation 1.11.

1.20 The turn-off gain predicted in Equation 1.18 indicates two conditions must be met to achieve the maximum gain in a PNPN gate controlled switch. The α_{NPN} must be high, and the sum of the α_{NPN} and α_{PNP} must be slightly greater than unity at the operating anode current level as shown in Figure 2. This relationship requires a device design that permits control of the equivalent transistor α's at high anode current levels.

1.30 The current gain of a transistor is composed of the product of the emitter efficiency (τ) and the base transport factor (β). W. M. Webster (2) shows a term for emitter efficiency affecting PNP transistor current gain in Equation 1.31.

$$\tau = \frac{\sigma_e L_e}{\sigma_b W (1 + Z)} \qquad 1.31$$

$$Z = \frac{W \mu_e I_e}{A D_p \sigma_b} \qquad 1.32$$

σ_b = conductivity of base

σ_e = conductivity of emitter

W = base thickness

L_e = electron diffusion length in emitter

I_e = emitter current

A = emitter area

D_p = hole diffusion coefficient

μ_e = electron mobility

Chih-Tang-Sah, R. N. Noyce and W. Shockley (3) report carrier recombination plays the dominant role in the determination of the emitter efficiency of forward biased junctions at low current level. The portion of the emitter current due to this mechanism consists of carrier recombination in the space charge region and thus is not available for transistor action. As the current is increased, the diffusion current dominates and the increased injected charge causes a small field to develop in the base region which aids the flow of injected carriers from emitter to collector. At high injection levels, the conductivity of the base region is increased and the volume recombination is increased resulting in a relative decrease in the emitter efficiency shown in Equation 1.31 and 1.32. The material lifetime becomes important in the determination of the low current emitter efficiency because of its effect on carrier recombination. Normally the τ can be assumed to be equal to unity if the impurity concentration of the emitter is high compared to the injected carrier density and impurity concentration of the base.

1.40 The transport factor (β) is primarily a function of the width of the base region and the material life time. Both base regions in a PNPN structure are conductivity modulated at high currents, and wide bases, high resistivity material necessary for high voltage devices contribute to an increasing β with increasing current. Geometry advantages may exist at high current densities due to base de-biasing effects allowing some control of the high current transport factor with various base structures.

1.50 The previous discussion has been concerned with an analysis of the design problems affecting transistor current gain at both low and high current levels. The increase in transistor α with current is partially due to recombination centers becoming saturated at high injection levels. This causes an effective increase in the device lifetime and therefore an effective increase in α. The equations given can be adapted for the equivalent NPN and PNP transistors, but the form presented in this analysis refers directly to the PNP structure. Normally the high current NPN α does not increase much with current since its low current value is close to unity and the impurity concentration of the P-base is high. The α of either equivalent transistor structure can be limited by increasing the ratio of base width to diffusion length. An analysis of the effects of high current on the PNP α shows that the PNP α can approach a reduced limit for wide N-base widths. This requires the assumption that recombination varies linearly with excess minority carrier concentration in the base region, and that life time and diffusion length are independent of injection level.

1.60 By examining the factors affecting the equivalent NPN and PNP transistor current gains, changes can be made in the composite PNPN design to optimize the device gate turn-off gain. The basic requirement for PNPN regeneration in order to maintain anode conduction is obtained from Equation 1.12. This shows that the sum of $\alpha_{NPN} + \alpha_{PNP} = 1$ for sustaining conduction. This point is related to the value of anode current I_h shown in Figures 2 and 3. Therefore at any anode current level greater than I_h, the sum of $\alpha_{NPN} + \alpha_{PNP} > 1$ and the α sum must be reduced below unity in order to achieve turn-off. The relationship of the gate controlled switch B_{off} to the equivalent transistor α's is given in Equation 1.18 and methods for controlling these alphas at high currents are discussed in the design requirements.

Design Requirements

2.00 The previous discussion on the theory of gate controlled switch operation pointed out three basic requirements for optimum B_{off} characteristics.

1) α_{NPN} should be high
2) α_{PNP} should be low
3) $\alpha_{NPN} + \alpha_{PNP}$ should be slightly greater than unity at the anode load current value

The B_{off} characteristics are emphasized in the design stage because no previous experience is available concerning high current-high gain gate controlled switches. However, three additional requirements are specified.

1) Voltage requirement

   $B_{vf} > 500$ volts

   $B_{vr} > 500$ volts

2) Current requirement

   $I_f = 10$ amps

3) Switching speed requirement

   $t_{off} \leqq 3$ µs at 500 volts and 10 amps

   t_{off} $P_w \leqq 5$ µs at 500 volts and 10 amps

The device structures necessary to optimize each individual requirement are not compatible with each other and considerable compromise is indicated.

2.10 The operating voltage specified requires a high resistivity N-base material to ensure adequate breakover characteristics. The theoretical discussion on multiplication factors indicated the differential between the operating voltage and the device breakover voltage should be maximum in order to maintain the gain characteristics with high voltage switching operation. The high resistivity N-base will also increase the α of the PNP structure which is an additional limitation on the B_{off} characteristics at high anode currents. The N-base width necessary to prevent a base voltage punch-through problem must be calculated from the maximum N-base resistivity specified. While some depletion layer movement will occur in the P-base region, this distance is normally minimum for effective conductivities (σ) greater than about 8.0 ohm-cm^{-1}. The minimum values calculated for the two base widths will be part of the determining factor for minimizing the device switching speed.

2.20 The device current requirement determines the minimum cathode area of the device. The minimum area for normal operation at 10 amps is calculated to be about 125×10^{-4} in^2. The actual base areas will be determined by the device geometry, but base de-biasing effects can become important for large area base regions. The design current limits the minimum package requirements, but the gate turn-off power and anode switching power subjects the device to additional power dissipation during switching operation. The 9/16" stud package was chosen to meet the power dissipation requirements.

2.30 The switching speed specified at the high voltage and high current level represents a considerable improvement in the relative speed capabilities of existing devices. It is recognized that compromises will be necessary for optimizing all parameters, but control of the device lifetime will be necessary to meet the desired speed. The optimum turn-on lifetime requirement is just opposite to the optimum turn-off life time requirement. Therefore effort should be made to preserve the lifetime in the P-base while controlling a reduction of lifetime in the N-base. The P-base region is a fairly high concentration diffused layer and lifetime will necessarily be poor, but any lifetime remaining will be advantageous to preserve. An additional benefit can be obtained from the high B_{off} characteristics in reducing the device storage time (t_s). As carriers are withdrawn from the P-base region during the turn-off interval, the storage time can be reduced affecting a reduction in the device turn-off time. Therefore for a specified reverse gate current during switching operation, a device with high B_{off} will have an effective increase in the amount of carriers withdrawn in relation to the minimum current required to turn-off the device. A compromise must be reached between the maximum N-base width required for high B_{off} and the minimum N-base width required for optimum switching speeds.

2.40 A minimum turn-off gain of 20 is specified at the anode conditions of 500 volts and 10 amperes. Considerable discussion has indicated the desirable

α relationships necessary to achieve this goal. Almost every device variable discussed has an effect on the turn-off gain of the structure. The device geometry itself has an effect on B_{off} through relative shifts in the current density pattern resulting in changes in the conductivity modulation of the base regions. All of the compromises necessary prompted considerable work to be expanded on investigating methods for controlling high current alpha structures.

Project Programs

3.00 The theoretical evaluation of the requirements necessary for control of high power gate controlled switch parameters resulted in outlining a three part program.

1) Lifetime Control Methods
2) Device Geometry Effects
3) Diffusion Technology

The first two parts of the program were aimed at acquiring basic information to allow control of high current alpha structures and optimize device switching speeds. The third part of the program was aimed at learning basic diffusion effects on the dynamic switching characteristics, the device power switching capabilities, and the anode saturation characteristics.

Lifetime Control

3.10 Investigation of lifetime control methods was reduced to two probable selections because of the minimum time available for extensive basic development work. Temperature quenching methods and gold doping techniques seemed to present the most logical solutions to the problem.

3.11 When a semiconductor material is heated to some uniform equilibrium temperature and then subjected to a rapid decrease in the equilibrium temperature, a degradation of the material lifetime will result. The decrease in the material lifetime is proportional to the rate of the decrease in quenching temperature. This method of selective lifetime control was recognized as a possible solution to the gate controlled switch B_{off} and switching speed problems. The lifetime degradation occurred throughout the entire structure when the rate of temperature decrease was uniform throughout the structure. It was discussed before why it was desirable to maintain the lifetime (τ) and α in the NPN structure while decreasing the τ and α in the PNP structure. Therefore, an effort was made to develop a process where the material could be subjected to a non-uniform quenching rate throughout the layers. The PNP structure was designed to have the higher quenching rate while the NPN structure was being quenched

at a reduced rate. Figure 4 shows the physical layout of the apparatus described. The material was loaded on a large thick piece of quartz with the P-emitter layer up. The quartz boat was connected to a screw transport with a long quartz rod. When the motor connected to the screw transport was started, the quartz boat with the semiconductor material could be moved from the high temperature furnace to a liquid nitrogen cooled helium manifold. By controlling the speed of the transport screw, the rate of the quenching action could be varied to a maximum speed of 4 sec withdrawal time from the furnace heat zone to the cooling manifold. The NPN structure was adjacent to a very good heat sink and therefore experienced very slow temperature changes. The PNP structure was positioned up in the quartz boat and during the quenching process was moved directly into the path of the cooling medium from the manifold. This combination action was believed to produce a non-uniform quenching rate desirable for the gate controlled switch device. Data was needed to determine if the quenching was non-uniform in its action, and the relative turn-on and turn-off time were chosen to provide this information. A summary of the results of this experiment is shown in Figure 5. A control run was included with four other groups of devices at various increasing quenching rates.

A comparison of the turn-on times showed almost no change from the control run to the most severe quenching rate. A comparison of the turn-off times showed a considerable decrease in the turn-off times above a quenching temperature of 1000°C. The B_{off} shows a general upward trend with increasing quench rate, and the device holding currents show a considerable increase from the control run value. The results could be interpreted to mean that the τ in the NPN structure was already so low because of the P-base region being a relatively high concentration diffused layer, that no additional change in the P-base τ was possible. To check this possibility additional quenching runs were made with uniform quenching rates. The average device turn-on time was about 1.25 times the turn-on time of the previous quenching series, and the device B_{off} was reduced. Both of these results indicate that non-uniform quenching rates are being achieved and a considerable improvement is possible in the device B_{off} and the turn-off times. However, the results of every quenching series made showed a marked decrease in the breakover characteristics of the device. The amount of degradation was found to be proportional to the rate of the quenching experienced. This result is explained by atomic dislocations and stresses being set up by the severe quenching rates used for the experimental runs.

3.12 The conclusions reached from the experimental data was that non-uniform lifetime control was possible. The device B_{off} and the switching speeds could be improved considerably, but the disadvantage of degradation of the breakover characteristics was too severe to make the method practical.

3.13 Gold doping experiments were started on bulk N-type material. The lifetime and ρ of the sample was measured and then Au was evaporated and diffused on the sample. The lifetime and ρ was measured again to determine the effects of gold diffusion and its effective penetration on N-type material. The actual Au diffusion constant reported by other groups (4) (5) were in disagreement and therefore some basic information was required to ensure lifetime control in the N-base region.

3.14 High concentration Au sources develop high ρ -layers when diffused into bulk material. These high ρ -layers appear to be skin effects and penetrate about 0.2 mils or less into the bulk material. The actual ρ of the skin layer is dependent upon the gold diffusion time and temperatures. When diffusion times are increased at a constant diffusion temperature, the maximum ρ of the skin layer will increase. Some typical samples showed an increase from 3.6 Ω cm to 11.0 Ω cm for a 10 min at 820°C diffusion. A similar sample showed an increase from 4.5 Ω cm to 59 Ω cm for a 30 min at 820°C diffusion.

3.15 Lifetime measurements on N-type bulk material showed an apparent reduction in lifetime with very little regard to the diffusion times and temperatures above a minimum value. Because of this result a series was started to determine if the lifetime degradation might be due to the heat treatment of the samples even though considerable care was taken to ensure slow cooling conditions. The samples were heat treated with no Au present in a furnace for 2 hours at 1200°C. The material was then furnace cooled and lifetime measurements were taken on all samples. The starting range of lifetime was considerable ($\approx$ 57-352 μs), and the final lifetime readings were all degraded to about the same value of 30 μs. The same samples were run through additional cycles described above to ensure the change in lifetime due to a heat treatment was not a continuing degradation - no additional changes in lifetime were noted.

3.16 It was recognized that lifetime control in bulk material due to Au doping techniques didn't necessarily reflect the results that would be achieved in multilayer structures. The measurements of PNPN Au doping series indicated three significant results. The device holding current and saturation voltage at high current increased with increasing Au diffusion times and temperature. The $I_{gt(off)}$ values decreased for constant load currents when the Au diffusion times and temperatures were increased. The previous lifetime measurements didn't support a continued change in β_{off} due to lifetime changes so measurements were made to determine the effects of Au diffusions on the impurity density of the N-base region. The results were obtained from a computer program designed to calculate the impurity distribution from capacitance - voltage measurements (6). Figure 6 shows the impurity density plotted with the total P-base N-base junction depletion layer widths on four runs of 10-12 Ω cm material using four different Au diffusion temperatures. Even though the distance shown on the graph is the total depletion layer width, it represents very nearly the distance in the N-base since the P-base concentration is fairly high compared to the N-base concentration. The results shown on the graph

can be directly related to the Au diffusion temperatures with the highest Au diffusion temperature corresponding to the lowest impurity density. The anode saturation characteristics are partially dependent upon the impurity density of the base, and the device surge characteristics can almost be predicted from the graph. The high impurity density device had surge currents greater than 75 amperes at 2 volts drop, and the low impurity density device had surge currents around 15 amperes at 2 volts drop.

3.17 The results discussed allowed the selection of an Au diffusion time and temperature dependent upon the device diffusion structure. The use of a gold doping technique provided a method of controlling the device lifetime and P-emitter efficiency. Neither one of the two parameters could be optimized due to the detrimental effects on other parameters, but a method was available to reach the optimum compromise with the other parameters.

Geometry Effects

3.20 Two geometry patterns are shown in Figures 7 and 8. Figure 7 shows an interdigitated geometry with a diffused base region surrounding the N-emitter region. This geometry was investigated to determine if any advantage existed over a concentric geometry because of the differences in the current density pattern affecting the base-conductivity modulation. Several runs were made with identical diffusions comparing the E-pattern and the ring-gate concentric pattern. Very little difference in the devices switching speed and B_{off} characteristics could be detected. However, there was invariably a lower anode breakover characteristics on the E-pattern devices compared to the ring-gate concentric devices. This was attributed to the presence of sharp corners on the square configuration together with the fact that the E-pattern was a scribed wafer rather than a cavitroned wafer. Another difference that was measured was the increased $V_{gt(off)}$ existing on the E-pattern devices. This could be explained partially by the increased distance involved from the gate area on the corner of the device to the cathode.

3.21 The concentric pattern was chosen in preference to the E-pattern, and initially devices with ring-gate configuration, shown in Figure 9, were measured. These devices exhibited satisfactory performance until measurements began on high voltage operation. All of the ring-gate concentric devices had a maximum power at which switching operation could be achieved without permanently degrading the device. The switching voltage limit was below the device breakover characteristics, and the current limit was well within the switching capabilities of the device at lower voltages. Investigation of the mode of failure found holes of various sizes in the geometric center of the N-emitter cathode area. This result is shown in Figure 10. The hole is about 5 mils in diameter. The cause of the holes was determined to be the same problem existing in power transistors operating in sweep applications. The device current goes through a

turn-off interval where the external gate source is forcing the device to turn-off transversely across the P-base layer. This results in the anode current being forced down to a finite area of conduction just prior to the instant of complete turn-off. When a ring-gate concentric geometry is used, this finite area becomes a point in the geometric center of the cathode area and the current densities in that point became tremendous. The high current densities cause very high temperature spikes and the material structure is ultimately destroyed.

3.22 The parallel-gate concentric geometry shown in Figures 8 and 11 was designed to minimize this effect. The two P-base gate regions are connected together to form a single gate terminal. This geometry does not solve the basic problem, but it does allow the turn-off area to be increased considerably since the finite area will now be a ring rather than a point. The actual comparison of the power switching capabilities of the two structures resulted in a marked increase in the power switching levels possible with the parallel-gate concentric geometry.

Diffusion Technology

3.30 The diffusion process designed to achieve the theoretical structure discussed under theoretical considerations is subject to several practical compromises. The device B_{off} characteristics cannot be optimized without sacrificing the anode voltage capabilities and the turn-off switching speed. While the Au doping studies provided a method of decreasing the compromise necessary, the anode saturation characteristics became a limiting factor for large Au doping levels. The Au doping effect on the impurity concentration in the N-base was discussed, and this effectively limits the minimum emitter efficiency of the P-emitter. A typical anode saturation characteristic is shown in Figure 12. The current magnitude of the knee of the characteristic is related to the emitter efficiency of either the P-emitter, N-emitter or both emitter efficiencies. While the emitter efficiencies can control the alpha structure; the N-base width itself can limit the maximum alpha value by an increase in the ratio of base width to diffusion length as described previously. As the N-base width is increased in order to increase the high current B_{off} of the device, the turn-off switching speed is also increased. It was determined that the minimum value of N-base width necessary to achieve the anode voltage characteristics specified would not allow the device to turn-off in the desired switching time interval without a severe limitation on the base lifetime. The base lifetime can be controlled over fairly broad limits, but a minimum value exists due to the requirement of the composite alpha sum being greater than unity to achieve the regenerative action for maintaining conduction. This represented an additional compromise necessary for high voltage, high speed operation.

3.31 The entire diffusion design is based upon the control of the composite DC alpha structures. The normal device has no connection to the N-base layer for measurement of the individual DC PNP and NPN alphas, and it is believed that four terminal measurements made in this manner give erroneous results due to current density crowding in the region of the contact. A method was adopted where AC alpha measurements can be made with the existing three terminals and then converted to DC alpha values (7). This method makes use of the normal difference in the cut-off frequencies between the NPN and the PNP structures. A plot similar to Figure 13 is obtained showing the relationship of the device frequency characteristics to the composite AC alpha. The upper frequencies can be related directly to the NPN AC alpha, and the lower frequencies can be related to the AC alpha sum. When the AC alphas are plotted to the individual transistor collector currents, the DC alphas can be obtained by two separate mathematical integrations. The DC alpha configurations of two devices from different experimental runs are shown in Figures 14 and 15. The holding currents can be predicted from the point that the α sum crosses the unity value even though there is a considerable difference in the holding current value of the two devices. The relative B_{off} of the two devices can be determined by measuring the slope of the α sum curve above the value of unity alpha. The higher the slope of the α sum curve, the lower the B_{off} of the device at high currents. These curves can be compared to the ideal case shown in Figure 2. A comparison of the curves for Figure 14 shows a reversal of the relative NPN and PNP alpha structures indicated in the ideal configuration. This is caused by a higher PNP lifetime, and the result is a lower B_{off} and a higher turn-off switching speed. The device shown in Figure 15 is closer to the ideal structure, but the device had a lower power switching capability. Figure 15 exhibited improved B_{off} and turn-off switching speed as the curves would predict. The actual currents plotted are in the region of the holding currents to show the accuracy of the system, but measurements at higher currents approach alpha values just slightly above the maximum alpha plotted.

3.32 The resultant diffused device is necessarily a compromise between the anode voltage capability, the turn-off gain, and the turn-off switching speed. The optimum compromise of the turn-off gain characteristics resulted in a B_{off} and anode current relationship shown in Figure 16. Devices with $B_{off} = 100$ at anode currents of 20 amperes have been observed, but the related parameters discussed above were not acceptable.

3.33 The dynamic switching characteristics of the gate controlled switch is very important in the determination of the turn-off power gain and the maximum power switching capability of the device. The switching dynamic impedance of the device is illustrated in Figure 17. The curve is a typical characteristic of the device gate - cathode dynamic impedance during the switching interval. A sine wave voltage is connected to the gate to cathode terminals, and the anode current is supplied from a DC source. The device is turned on in the positive half cycle sine wave input, and the gate-cathode voltage and current relationships are observed as the applied sine wave input starts negative. The

slope of the gate-cathode voltage-current curve during the reverse gate bias and prior to turn-off is defined as the switching dynamic impedance. A reduction in the magnitude of the slope of this curve allows a reduction in the input power required to turn-off the device. The ability of the device to switch high power anode levels is also related to this parameter. As the switching dynamic impedance is reduced, the power switching capability of the device is increased. The control of the dynamic switching impedance is achieved through control of the P-base and N-emitter concentrations. By limiting the N-emitter concentrations the dynamic impedance may be reduced, but a compromise must be made with the anode saturation characteristics and the device B_{off}. The NPN DC alpha curve of Figure 14 shows the effect of a reduction in the N-emitter efficiency on the NPN alpha to achieve good dynamic impedance characteristics.

3.34 The anode switching characteristics are a result of the control of the device base widths and lifetimes. The switching speed specification required a turn-off time of 3 μs with an anode condition of 500 volts and 10 amperes. The device turn-on time was not specified but an effort was made to maintain reasonable turn-on times in relation to the device turn-off times. By decreasing the N-base width, the turn-off time may be reduced, but a minimum width exists because of the high voltage depletion layer movement in the N-base. As the applied voltage is increased during switching operation, the depletion layer width is increased and this results in an increased turn-off switching speed. The variation in the anode voltage with turn-off time at a constant anode current is shown in Figure 18. This curve shows the optimum compromise obtained without severely limiting the other parameters required. The anode current relationship to the turn-off switching speed at a constant anode voltage is shown in Figure 19. A decrease in the base lifetimes will decrease the switching speeds shown in Figure 19, but a minimum value exists before the anode saturation voltage and the turn-on switching speed became unacceptable. The switching speed values shown on both of these curves can be altered by changing the gate drive current (I_{gr}) in relation to the minimum gate current $I_{gt(off)}$ required to turn the device off at the stated anode conditions. The relationship of the ratio of $I_{gr}/I_{gt(off)}$ to the turn-off switching speed is shown in Figure 20. The dominant change in switching speed due to a change in the gate drive ratio is shown to be a change in the device storage time. The storage time interval can become almost as long as the input pulse width for ratios approaching unity. While the optimum ratio for operation with 10 amps anode current appears to be a ratio of around 3, the optimum ratio is decreased with reduced anode current values.

Device Fabrication

4.00 The fabrication flow chart shown in Figure 21 gives a step by step description of the process developed. The slices are cleaned initially and a Gallium diffusion is made from both sides of N-type parent material. An alignment pattern shown in Figure 22 is put on the diffused slice to allow successive

registration of the patterns. After the P-emitter diffusion, the N-emitter pattern shown in Figure 23 is put on the slice and the emitter diffusion made. After the Au doping step, the plating mask (Figure 24) is put on the diffused material and nickel plated. The slices are then mounted and aligned for the cavitron step using the jig shown in Figure 25. After cavitroning, the individual wafer shown in Figure 26 is cleaned and mounted on a silver disc. The soldered device is shown in Figure 27. The completed cell is then etched, cleaned and surface protection applied. After a curing step is complete, the cell is mounted on the stud and canned and crimped. The leads are welded and the finished package outline is shown in Figure 28. The device is final tested, plated and symbolized as shown in Figure 29.

Evaluation Results and Test Equipment

5.00 The device evaluation measurements were made on existing test equipment with the exception of the power switching speed measurements. This equipment is pictured in Figure 30 and the schematic shown in Figure 31. The equipment was used for evaluation measurements during the development stages and characterization of the final design. The device power switching rating was established at 400 volts anode voltage and 10 amperes anode current. This gives a possible turn-off power gain control equal to:

$$G_{pwr} = \frac{V_{anode} \times I_{anode}}{V_{gt(off)} \times I_{gt(off)}} = \frac{400 \times 10}{0.5 \times 0.400} = 20,000$$

The devices characterized had an average t_{off} time of 6.5 μs with a minimum turn-off time of 3.9 μs observed. The turn-on time averaged 3.0 μs with a minimum turn-on time of 0.40 μs observed. All of the switching measurements were made with anode conditions of 400 volts and 10 amperes. Figure 32 shows an oscilloscope picture of a device turning on 400 volts to 10 amperes. Figure 33 shows the turn-off time with the same anode conditions. Both pictures have the gate current characteristics superimposed on the anode characteristics.

5.10 The device B_{off} characteristics are obtained in the test equipment shown in Figure 35. The anode source is a high current DC power supply, and the gate source is a variable AC voltage. The device is turned on and off at a 60 cps rate, and the gate voltage-current relationship is observed on an oscilloscope. A typical gate characteristic is shown in Figure 34. The vertical scale is instantaneous gate voltage, and the horizontal scale is instantaneous gate current. The low dynamic impedance is noted where the device turns off with a $\Delta V_{gt(off)}$ less than the gate-cathode potential due to the conduction current. This results in an instantaneous positive gate-cathode potential at the point of turn-off.

5.20 The thermal impedance of the device was measured on the equipment pictured in Figure 36. The maximum junction temperature following the conduction period was investigated in order to determine the maximum thermal impedance value. The device is required to regain its blocking characteristics within the turn-off time of the anode, therefore the junction temperature must not be allowed to exceed its maximum blocking values. The maximum thermal impedance of the device was found to be 3.0°C/watt. The maximum junction temperature of the device is 125°C. Since the reverse gate current is required to be applied during the turn-off switching interval, the maximum total power dissipation of the device is rated at 20 watts for a stud temperature of 65°C. The total power includes the sum of the product of the DC switching current and the saturation voltage plus the average product of the actual gate reverse current and gate reverse voltage. This requirement means as the operating frequency is increased and the reverse gate power becomes significant, the operating stud temperature should be decreased by additional heat sink area.

5.30 The high voltage-low current anode measurements are made on equipment shown in Figure 37. The equipment consists of a simple curve tracer anode circuit and a variable DC gate source for measuring gate saturation currents and voltages. The schematic for this test set is shown in Figure 38. The anode single cycle surge measurements were made on the equipment shown in Figure 39. This test set provides adjustable anode currents, and the instantaneous device voltage drop is measured on an oscilloscope.

5.40 Figure 40 shows a summary of the final test parameters recorded on the 45 devices delivered to George C. Marshall Space Flight Center for completion of the contract.

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Proceedings of IRE - September 1956

(2) W. M. Webster
On the Variation of Junction Transistor Current Amplification Factor with Emitter Current
Proceedings of IRE - June 1954

(3) Chih-Tang Sah, R. N. Noyce, W. Shockley
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Proceedings of IRE - September 1957

(4) W. R. Wilcox, T. J. LaChapelle
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Paper Presented Electro-Chemical Society - May 1962

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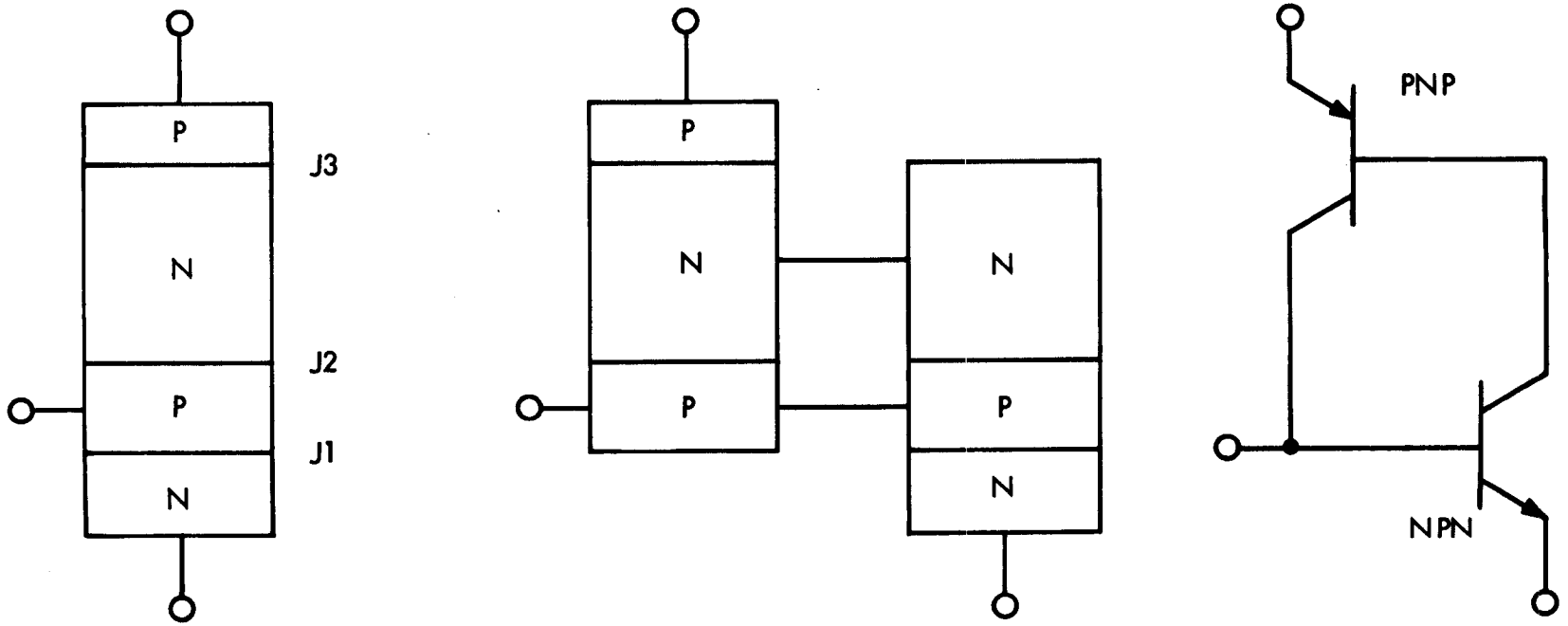
Solubility and Diffusivity of Gold, Iron and and Copper in Silicon
Journal of Applied Physics, vol. 27 - December 1956

(6) J. Hilibrand, R. D. Gold
Determination of Impurity Distribution in Junction Diodes from Capacitance - Voltage Measurements
R.C.A. Review

(7) W. Fulop
Three Terminal Measurements of Current Amplification Factors of Controlled Rectifiers
To Be Published

Conclusions

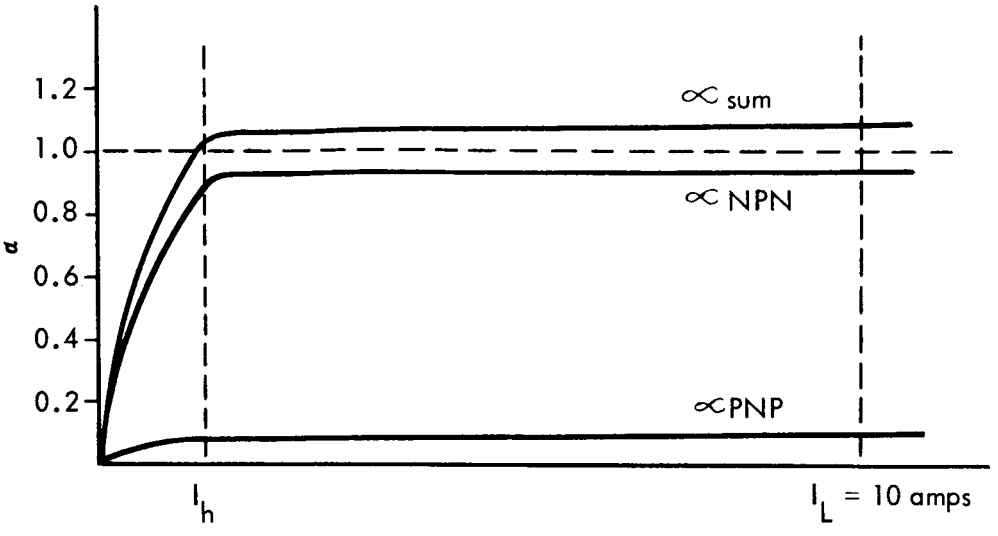
The contract specifications called for voltage, gain and speed requirements beyond any device capability presently available. Results from experimental runs indicated the feasibility of the individual contract parameters, however the final device design represented a compromise since some of these parameters could only be met at the expense of others. The 400 volt - 10 ampere switching device presented here is the best compromise available without severe limitations on the remaining parameters. The fifty prototype devices delivered to NASA are capable of switching 400 volt - 10 ampere DC loads with a typical B_{off} of 25 at 10 amps.



PNPN TRANSISTOR ANALYSIS

FIGURE 1

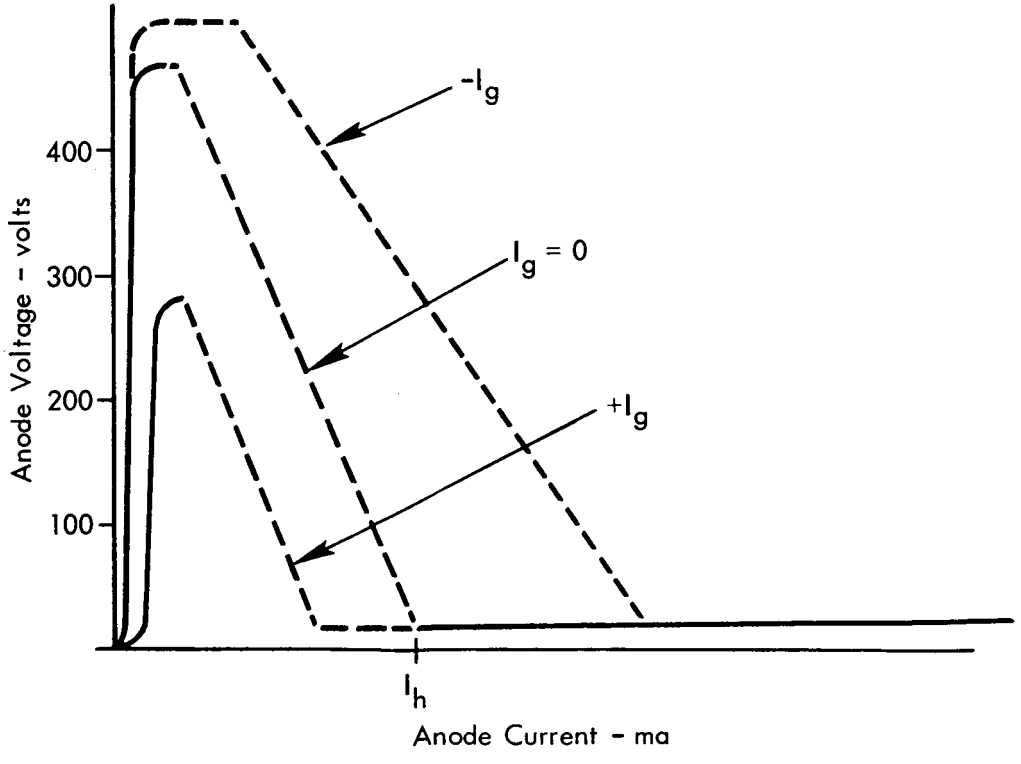
PNPN ALPHA CONFIGURATION



Anode Current - amps

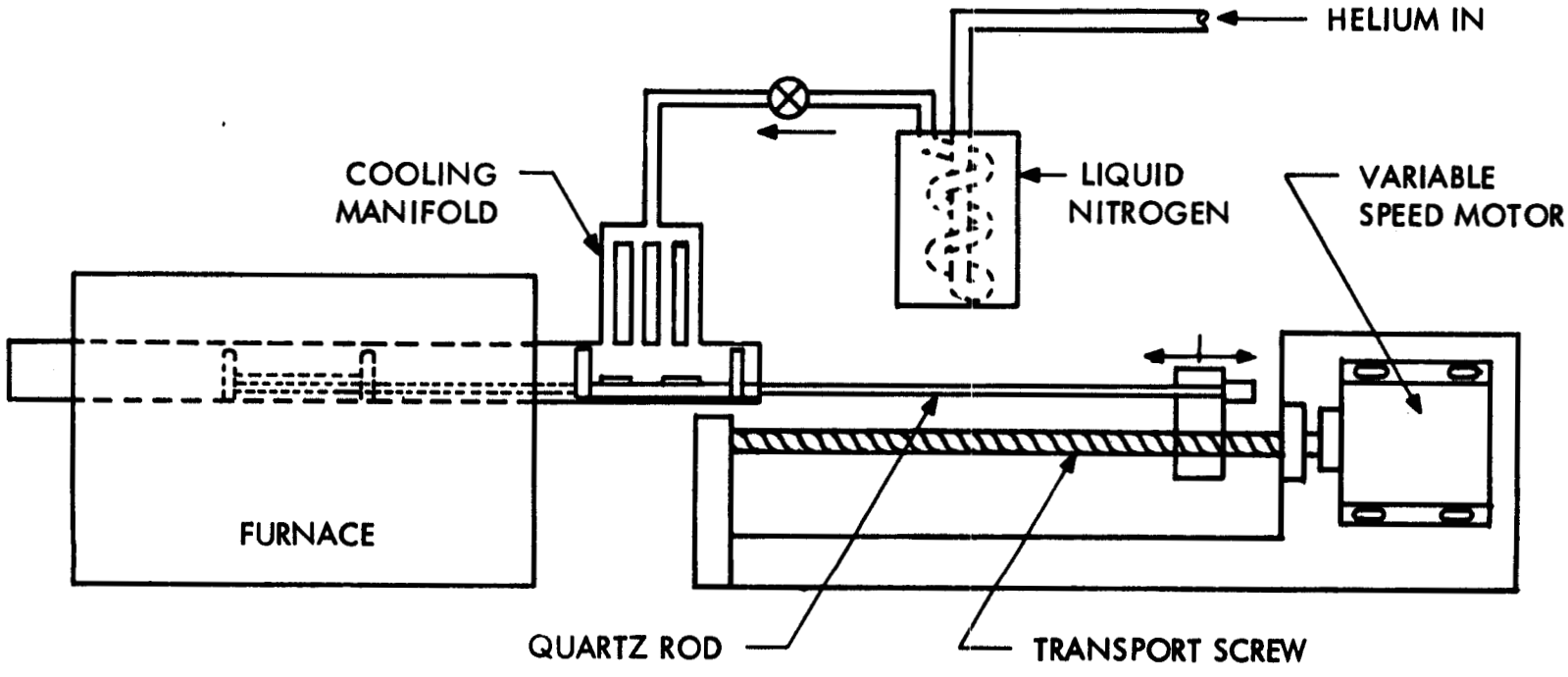
FIGURE 2

ANODE EI CHARACTERISTICS



Anode Current - ma

FIGURE 3



QUENCHING APPARATUS

FIG. 4

TI-2908 DATA SHEET (16-25) FIG. 5

TAKEN BY | DATE 12/13/62 | PAGE OF 1

Parameter Distributions of Quenching Runs

Run No.	Device Configuration	Quench Time (sec)	Quench Temp. (°C)	B_{vf} (Volts)	B_{vr} (volts)	I_h (ma.)	β_{off}	$V_{gt(off)}$ (volts)	t_d/t_{on}	t_s/t_{off}	$V_t/@I_t$
N 11	Concentric Parallel Gate	Control	Run	375	500	<.1	5.0	−9.0	.30/.60 μs	5.0/9.0 μs	2.9 V/75 ma
N11A-1	Concentric Parallel Gate	4.0	700	375	500	<.1	5.5	−10.0	.30/.55 μs	5.5/8.6 μs	2.0 V/75 ma
N11A-10	Concentric Parallel Gate	4.0	1000	250	500	1.0	8.0	−8.0	.30/.60 μs	4.3/7.0 μs	2.0 V/75 ma
N11A-13	Concentric Parallel Gate	4.0	1100	200	500	20.0	12.0	−7.5	.30/.55 μs	.40/.60 μs	2.0 V/75 ma
N11G	Concentric Parallel Gate	4.0	1200	150	200	60.0	16.6	−6.0	.30/.60 μs	.50/.60 μs	2.0/30 ma

DEPLETION LAYER
IMPURITY DISTRIBUTION

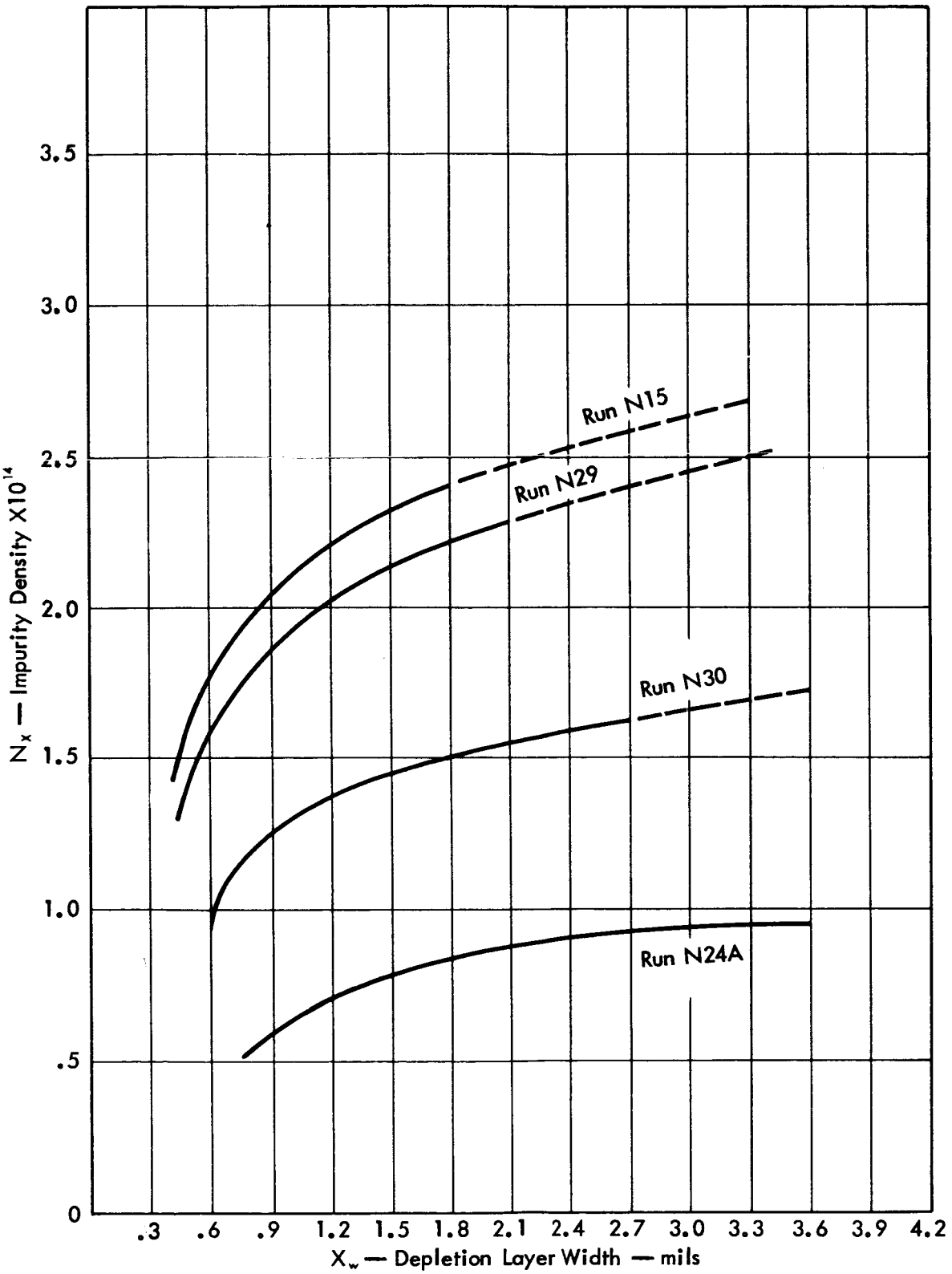


FIG. 6

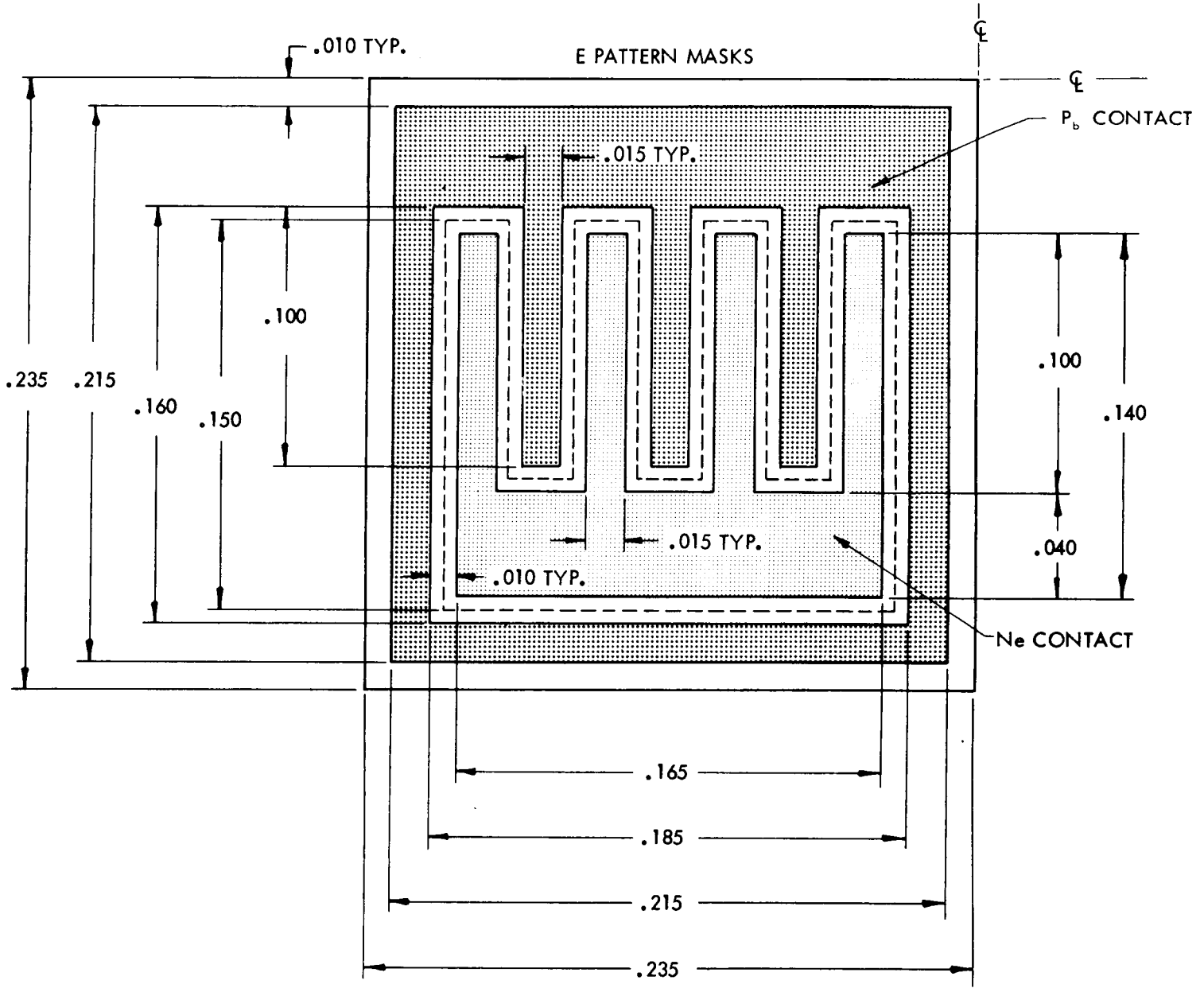
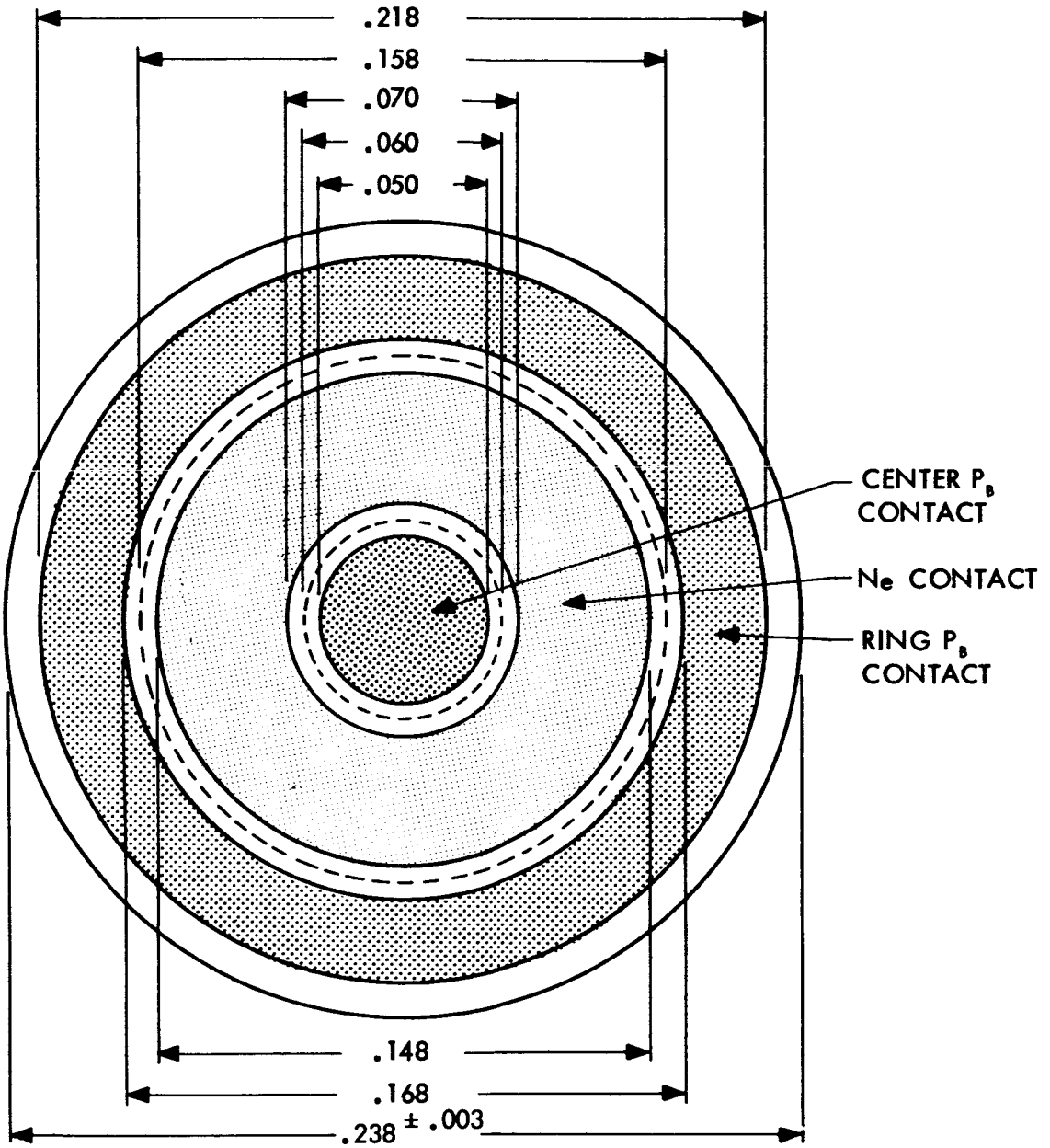

.010 TYP.
E PATTERN MASKS
℄
℄
P_b CONTACT
.015 TYP.
.100
.235
.215
.160
.150
.100
.140
.040
.015 TYP.
.010 TYP.
Ne CONTACT
.165
.185
.215
.235

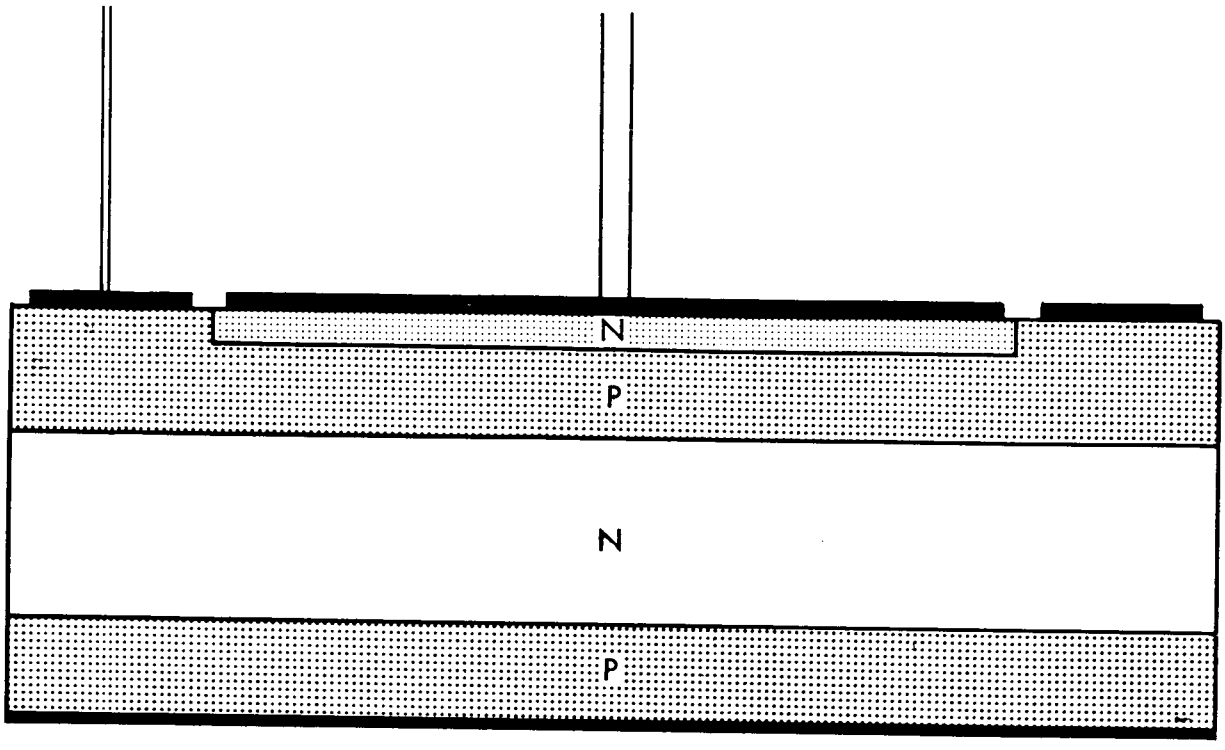
FIG. 7

CONCENTRIC PARALLEL GATE MASKS



NOTE:
DOTTED CIRCLES INDICATE DIFFUSED JUNCTIONS.

FIG. 8

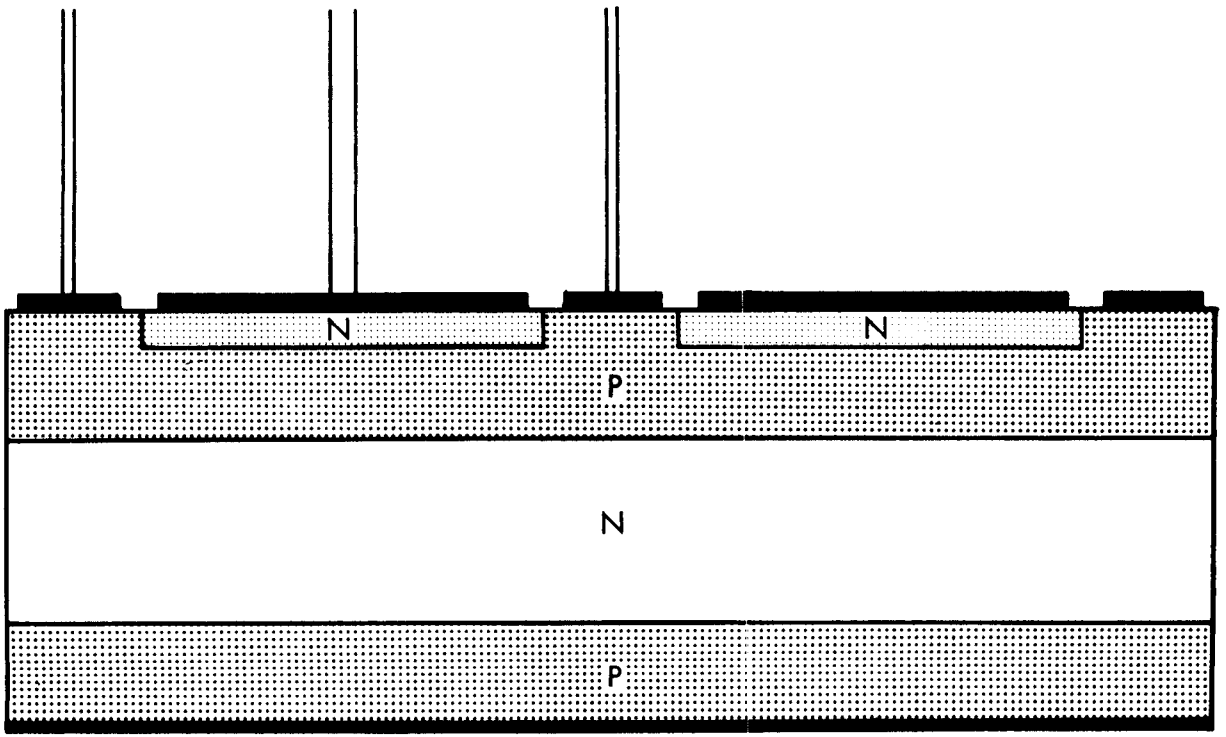


RING GATE DEVICE STRUCTURE

FIG. 9

POWER SWITCHING MATERIAL DAMAGE

FIG. 10



PARALLEL GATE DEVICE STRUCTURE

FIG. 11

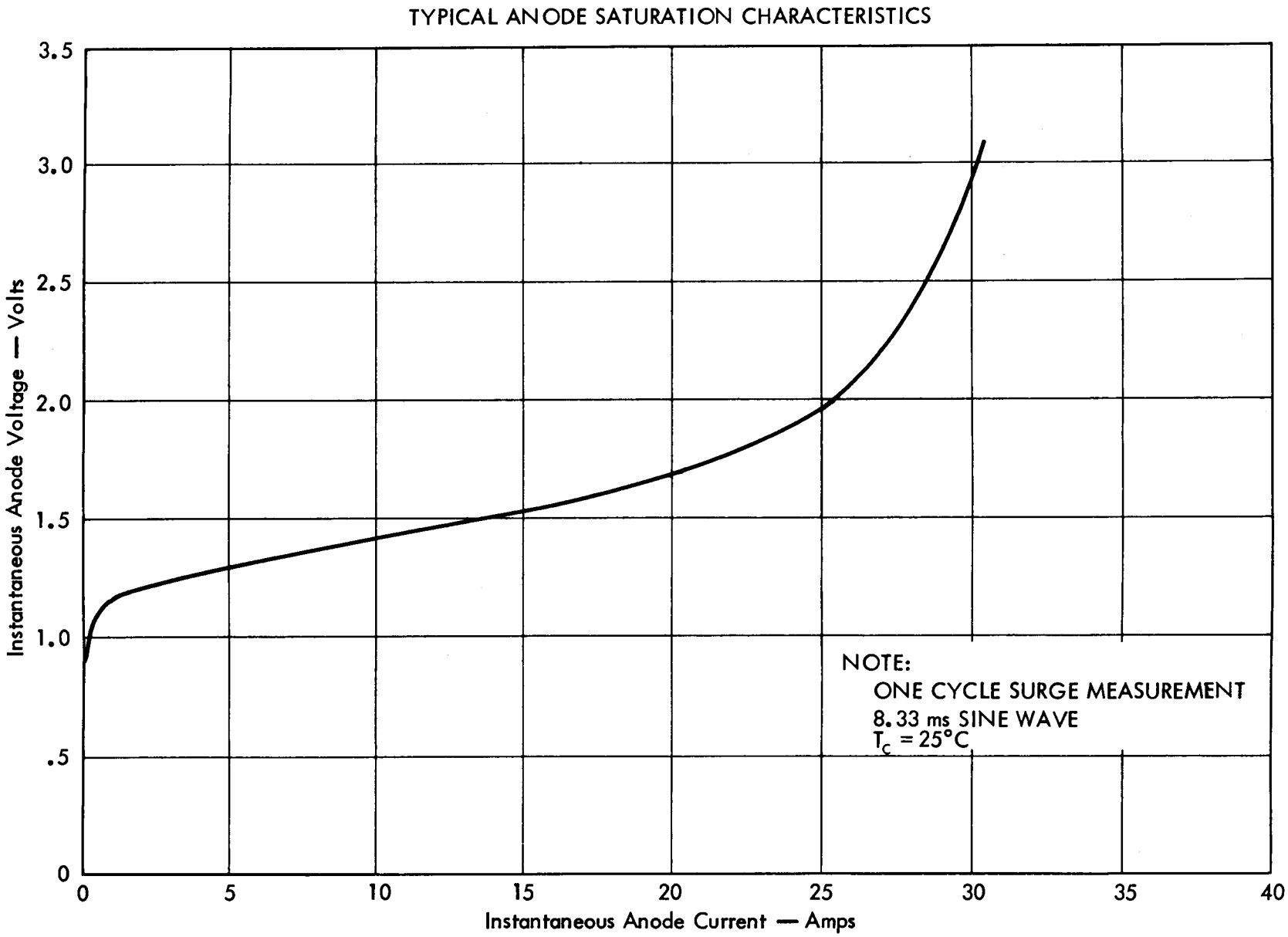

TYPICAL ANODE SATURATION CHARACTERISTICS
Instantaneous Anode Voltage — Volts
3.5
3.0
2.5
2.0
1.5
1.0
.5
0
0
5
10
15
20
25
30
35
40
Instantaneous Anode Current — Amps
NOTE:
ONE CYCLE SURGE MEASUREMENT
8.33 ms SINE WAVE
T_C = 25°C

FIG. 12

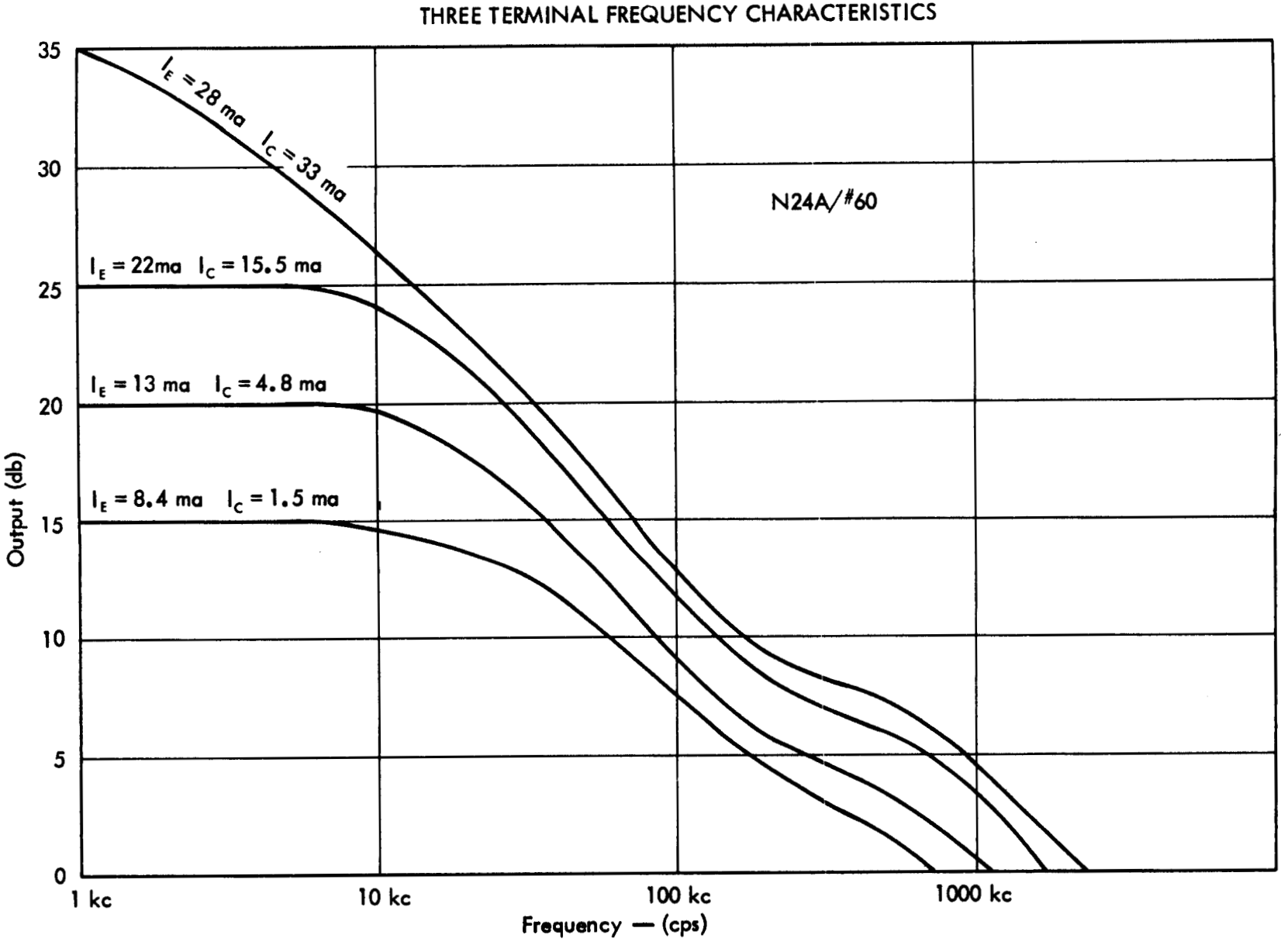

THREE TERMINAL FREQUENCY CHARACTERISTICS
35
30
25
20
15
10
5
0
Output (db)
I_E = 28 ma I_C = 33 ma
N24A/#60
I_E = 22ma I_C = 15.5 ma
I_E = 13 ma I_C = 4.8 ma
I_E = 8.4 ma I_C = 1.5 ma
1 kc
10 kc
100 kc
1000 kc
Frequency — (cps)

FIG. 13

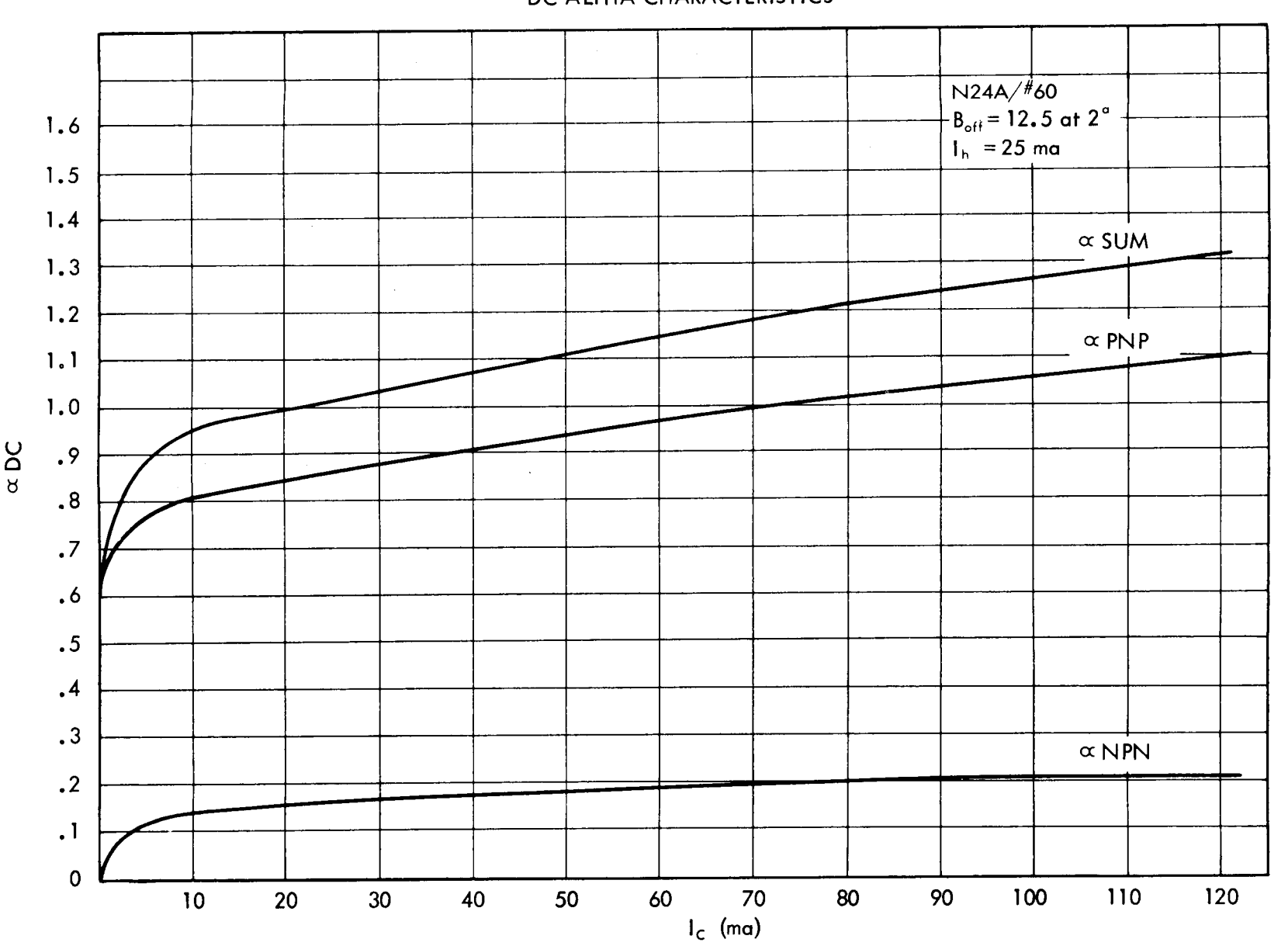

DC ALPHA CHARACTERISTICS
N24A/#60
B_{off} = 12.5 at 2°
I_h = 25 ma
∝ SUM
∝ PNP
∝ NPN
∝ DC
1.6
1.5
1.4
1.3
1.2
1.1
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
10
20
30
40
50
60
70
80
90
100
110
120
I_c (ma)

FIG. 14

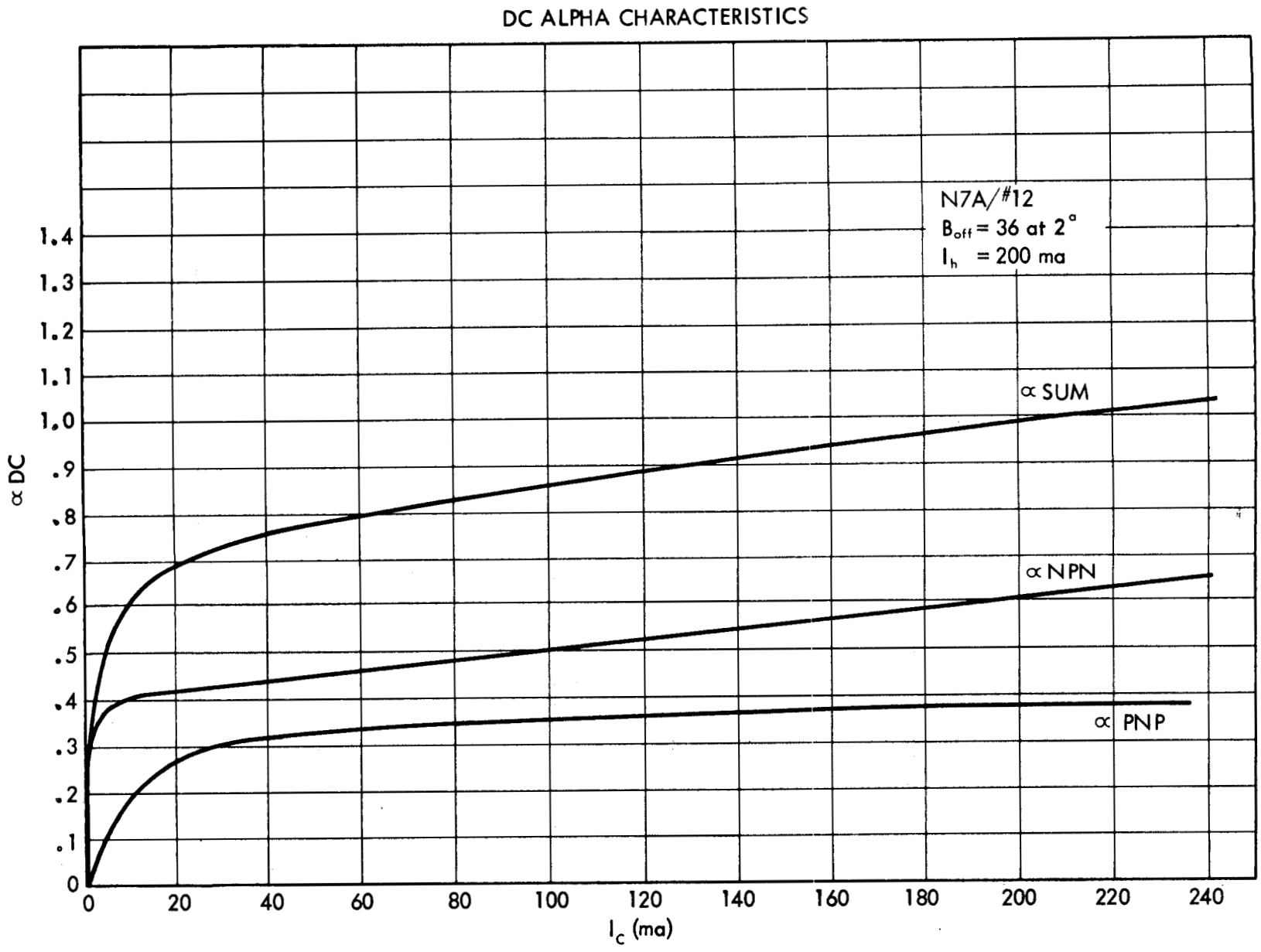

DC ALPHA CHARACTERISTICS
N7A/#12
B_{off} = 36 at 2°
I_h = 200 ma
∝ SUM
∝ NPN
∝ PNP
∝ DC
1.4
1.3
1.2
1.1
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
0
20
40
60
80
100
120
140
160
180
200
220
240
I_c (ma)

FIG. 15

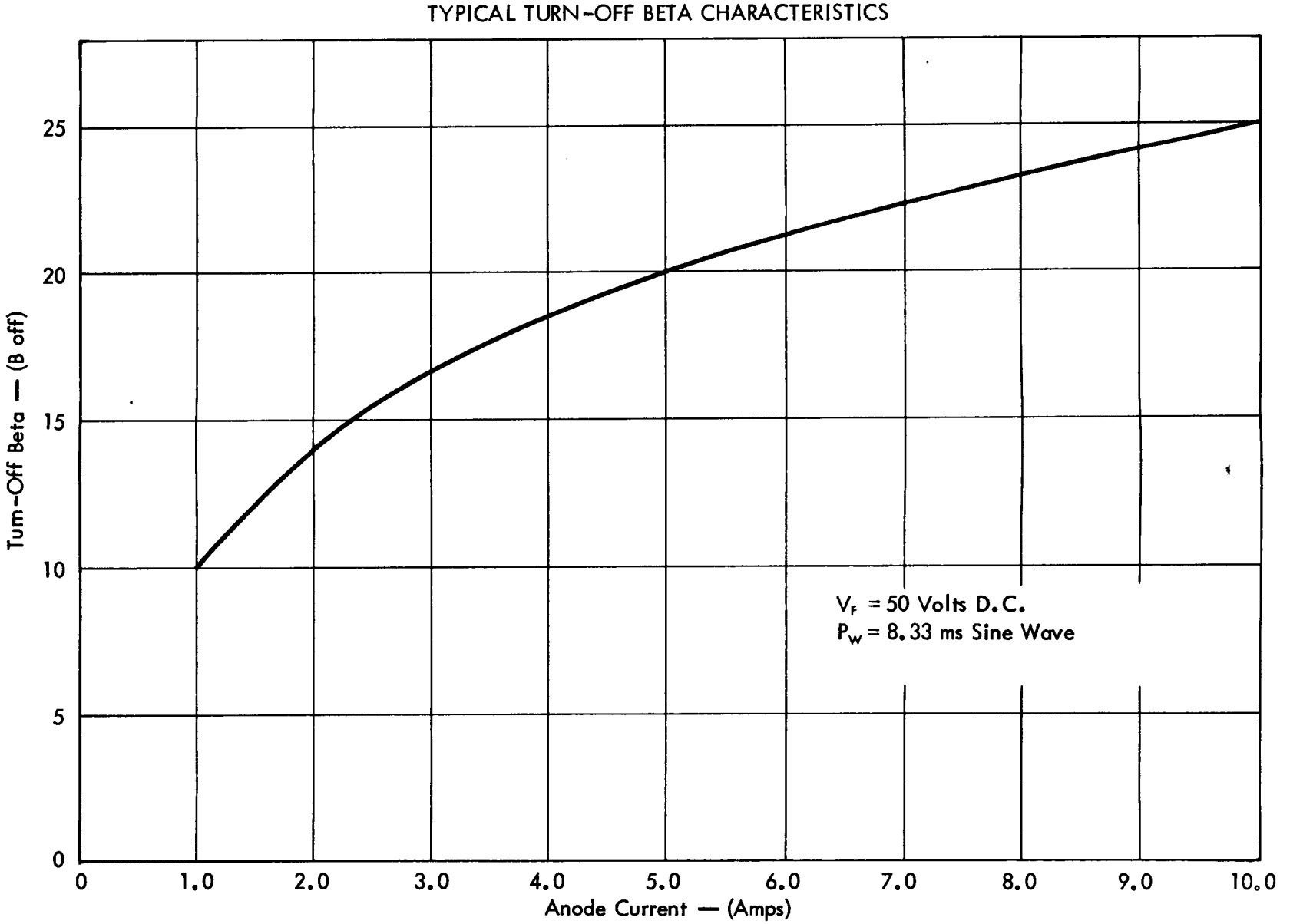

TYPICAL TURN-OFF BETA CHARACTERISTICS
Turn-Off Beta — (B off)
25
20
15
10
5
0
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
Anode Current — (Amps)
V_F = 50 Volts D.C.
P_W = 8.33 ms Sine Wave

FIG. 16

TYPICAL GATE SWITCHING CHARACTERISTICS

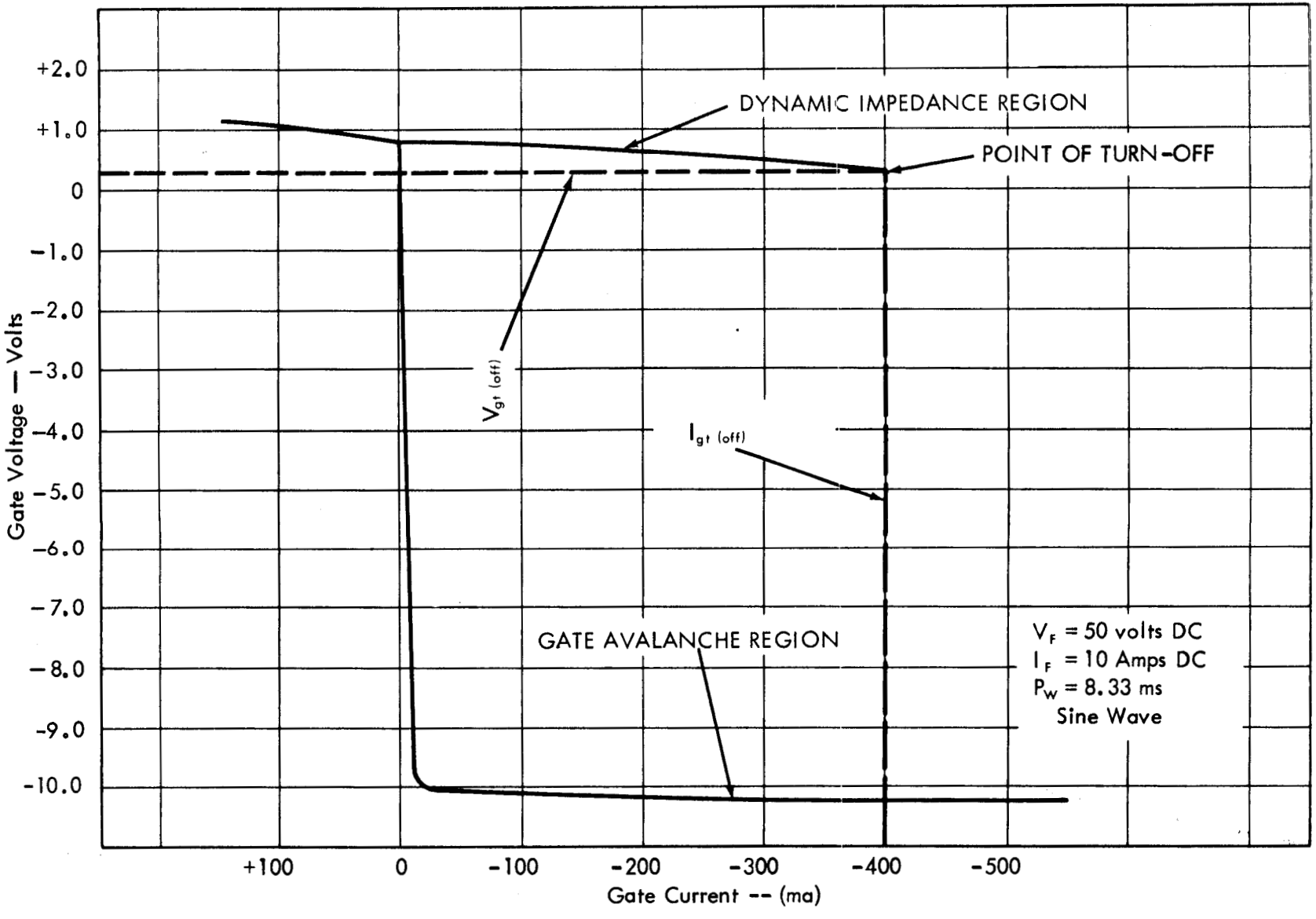


FIGURE 17

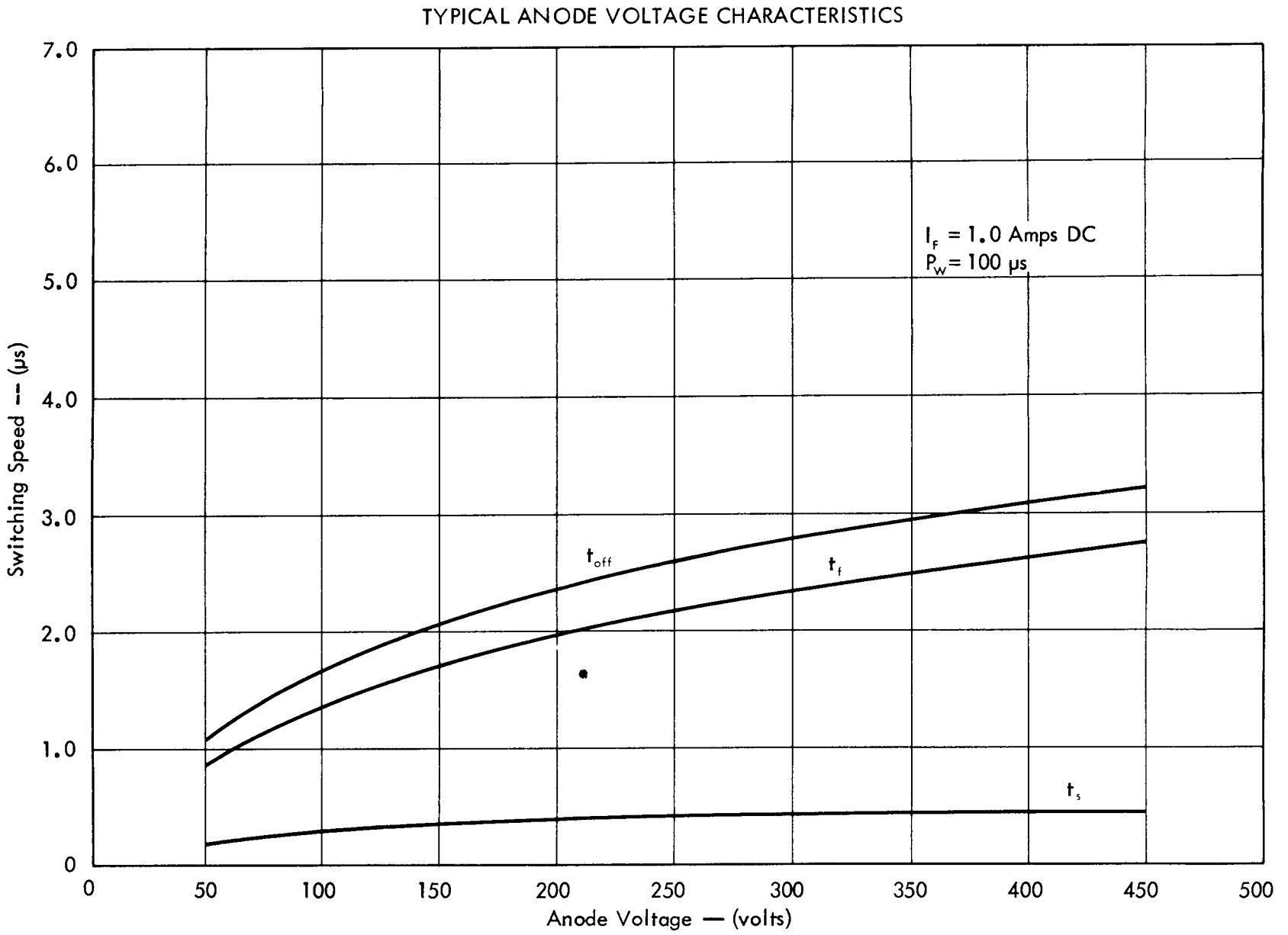

TYPICAL ANODE VOLTAGE CHARACTERISTICS
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0
Switching Speed -- (μs)
I_f = 1.0 Amps DC
P_W = 100 μs
t_{off}
t_f
t_s
0
50
100
150
200
250
300
350
400
450
500
Anode Voltage — (volts)

FIG. 18

TYPICAL ANODE CURRENT CHARACTERISTICS

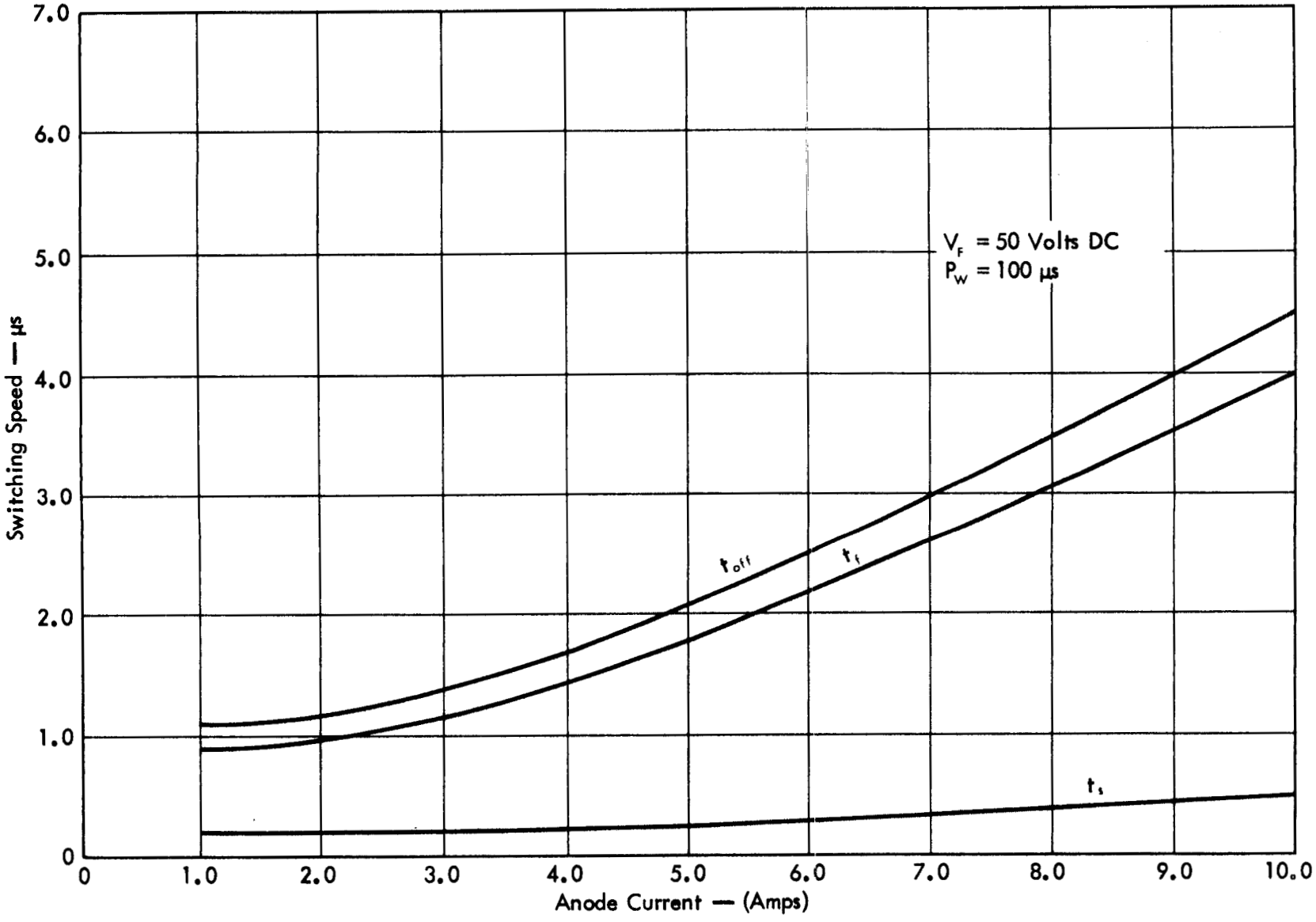


FIG. 19

TYPICAL TURN-OFF SWITCHING CHARACTERISTICS

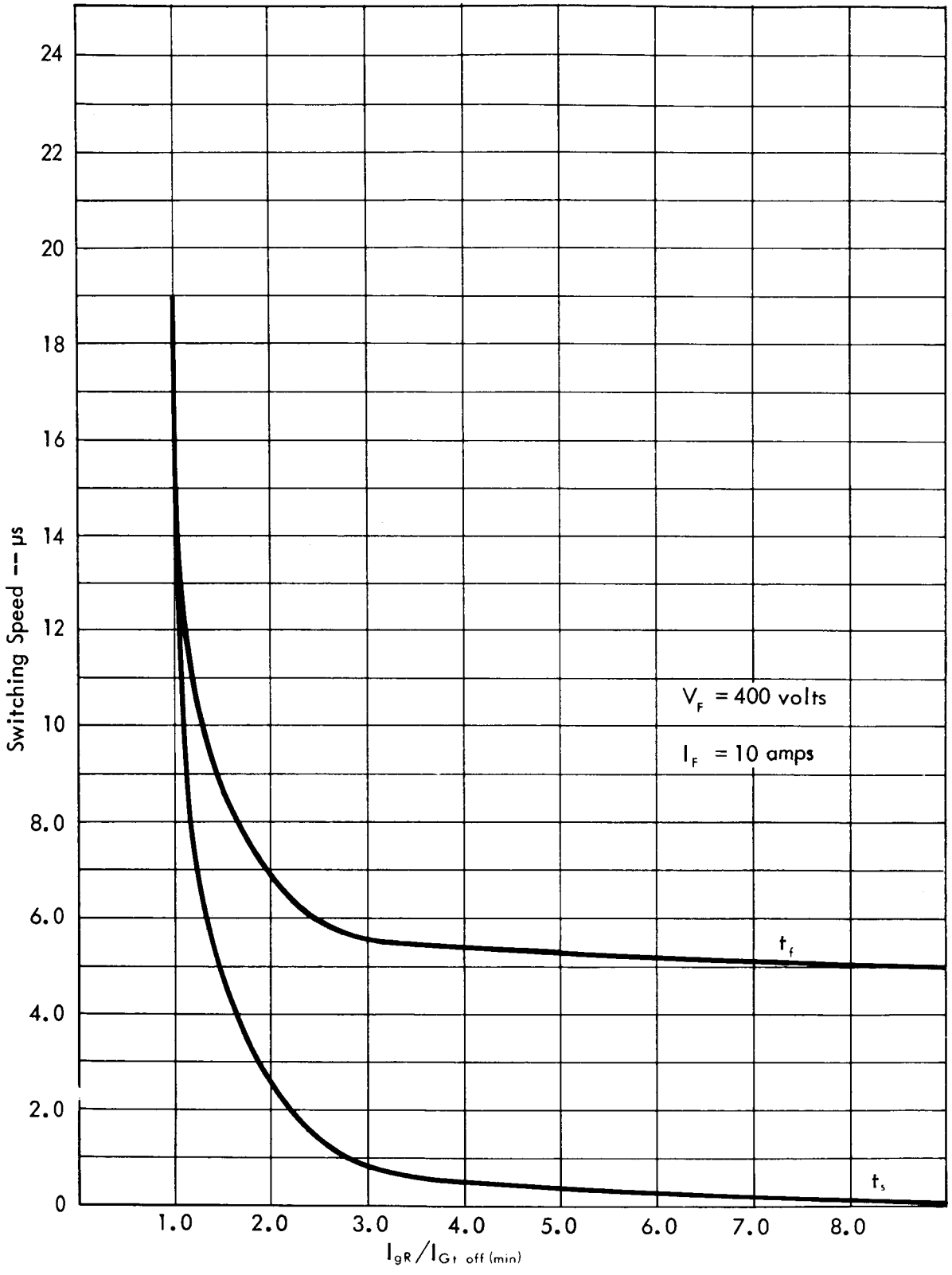


FIG. 20

10 Amp - GCS FLOW CHART

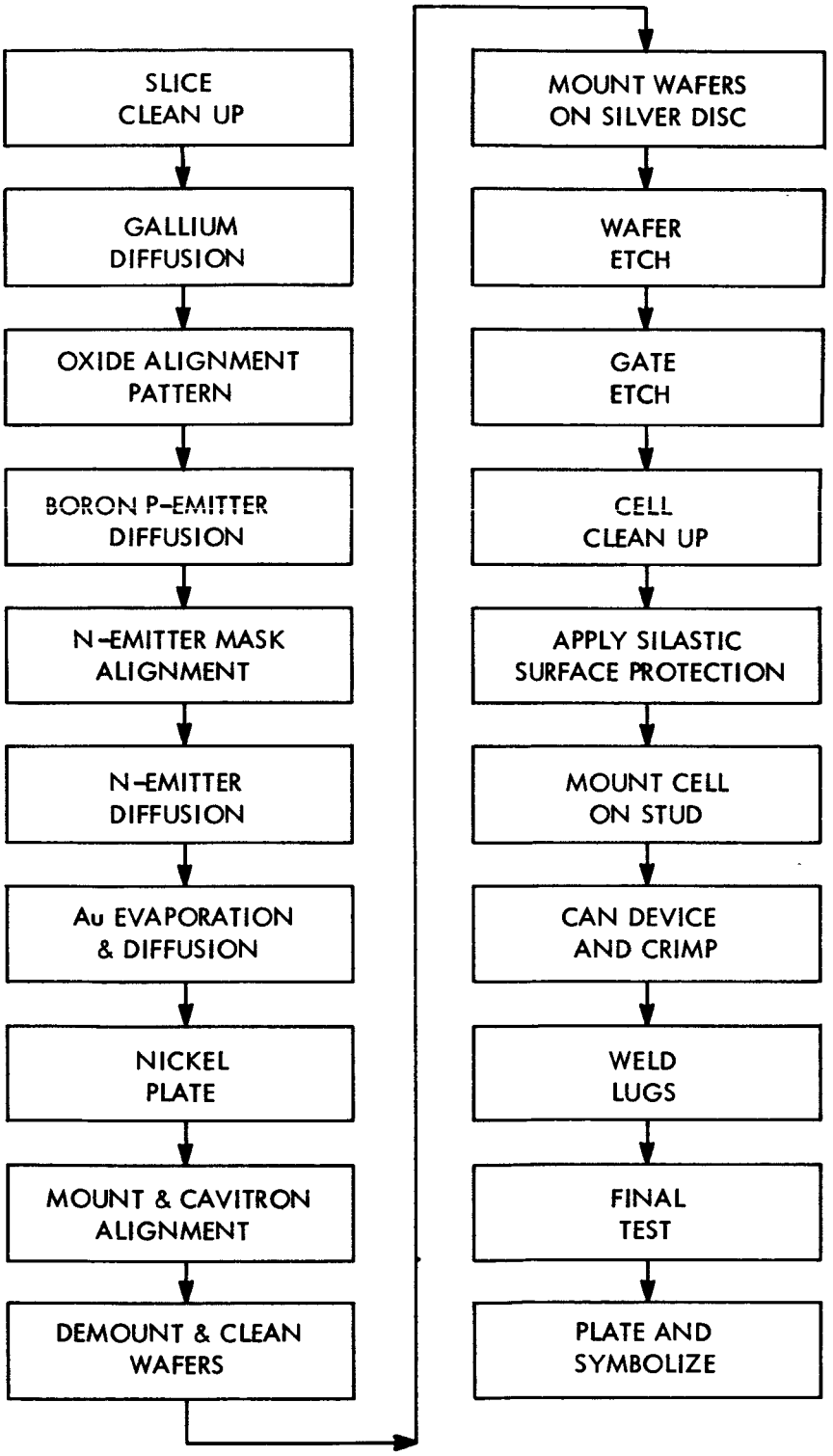
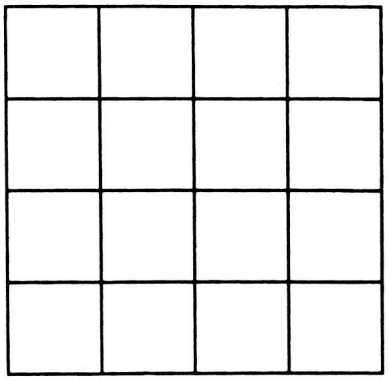
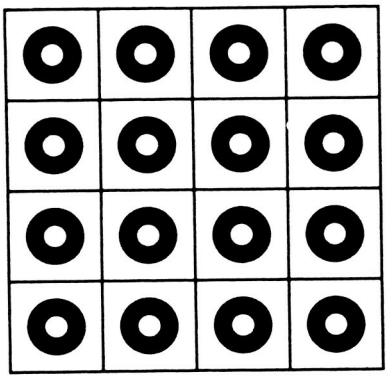


FIG. 21



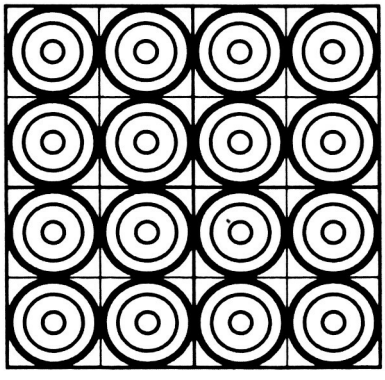
ALIGNMENT MASK

FIG. 22



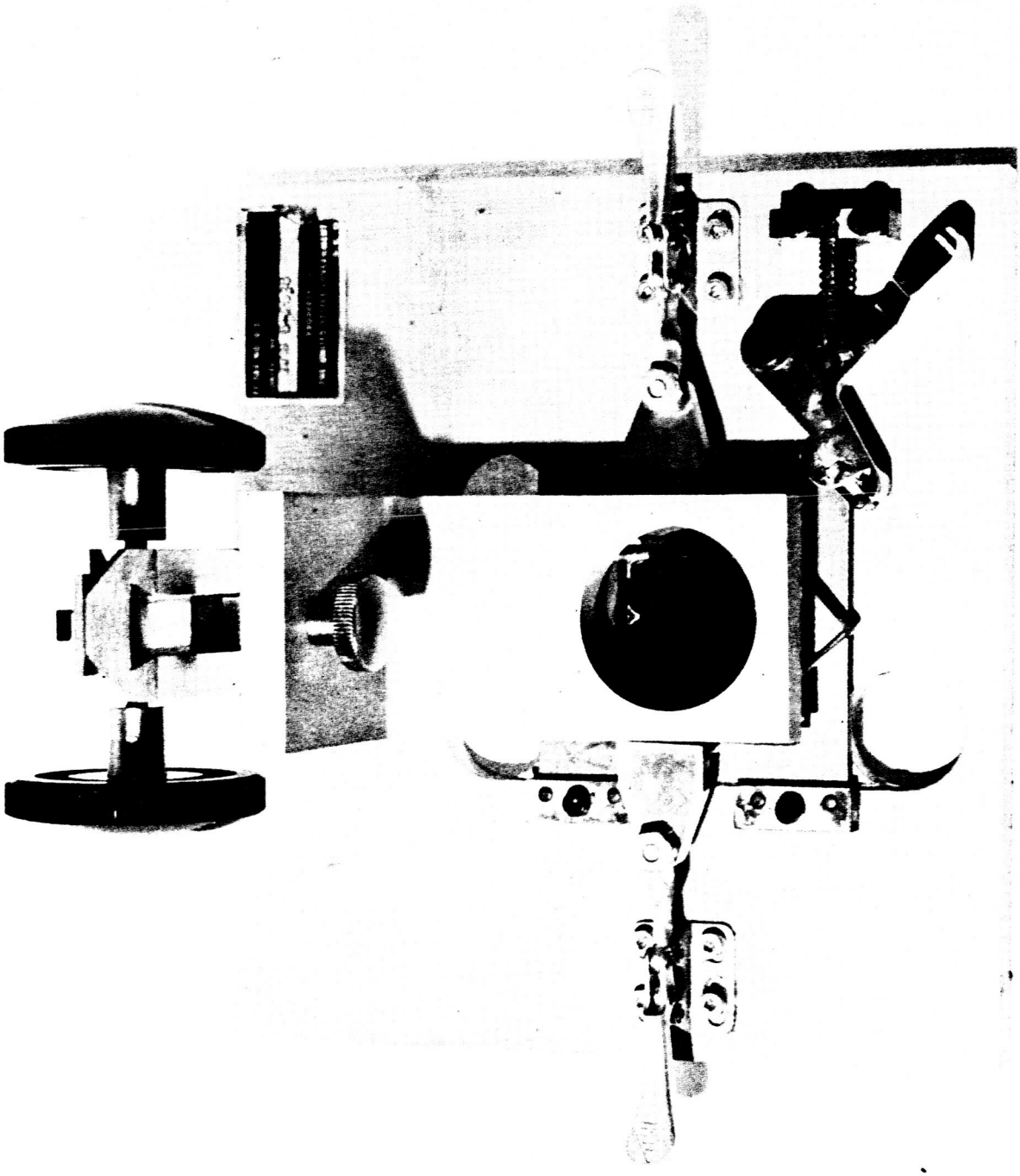
N-EMITTER MASK

FIG. 23



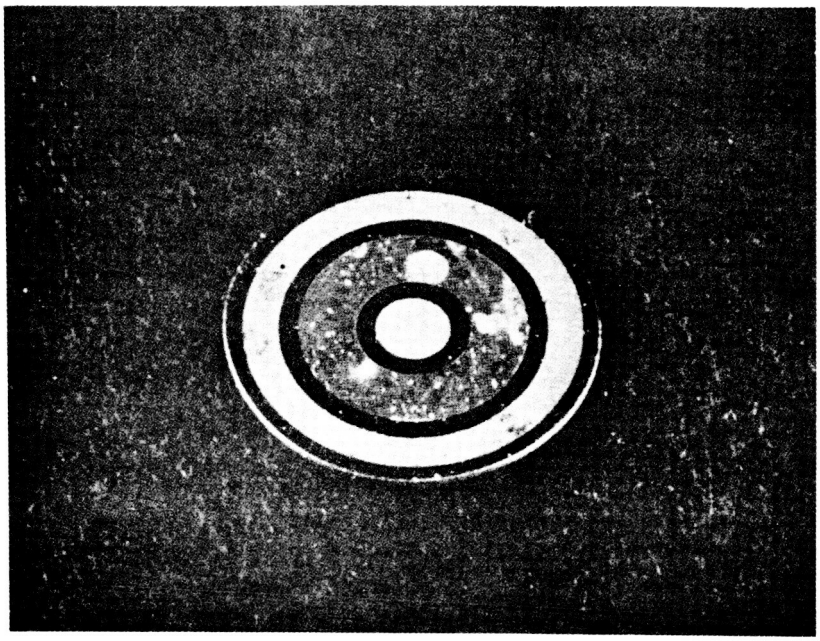
OXIDE PLATING MASK

FIG. 24



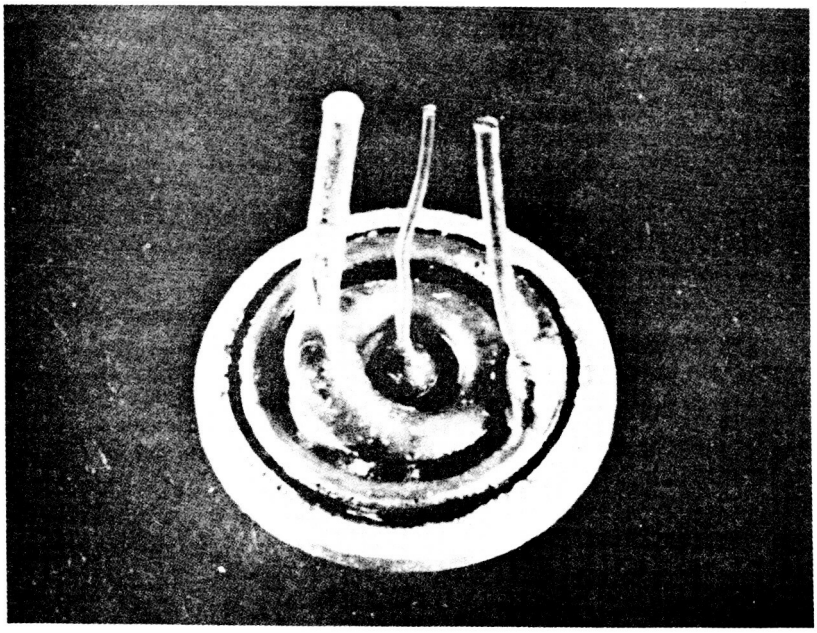
ALIGNMENT JIG

FIG. 25



CAVITRONED WAFER

FIG. 26



SOLDERED CELL

FIG. 27

DEVICE PACKAGE OUTLINE

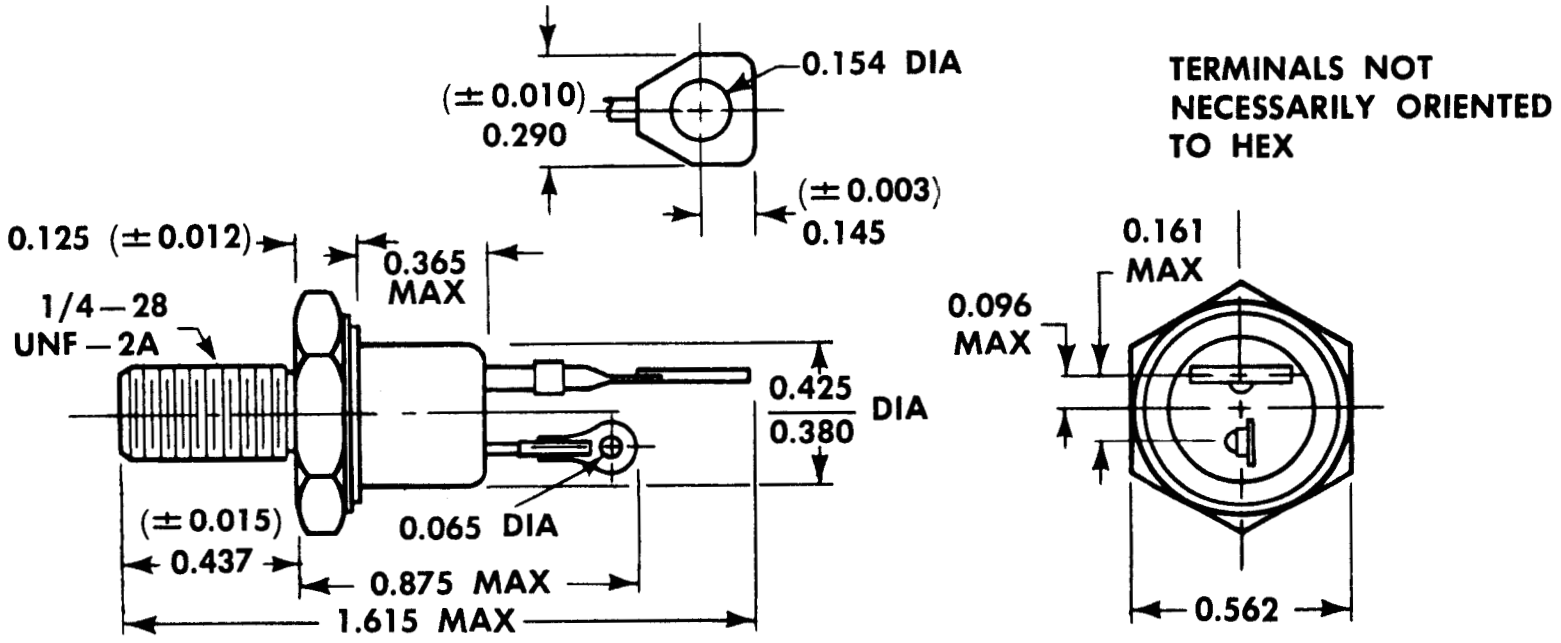
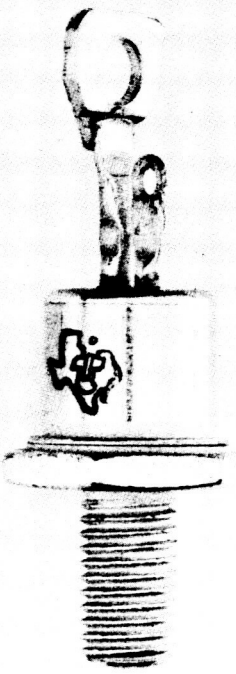
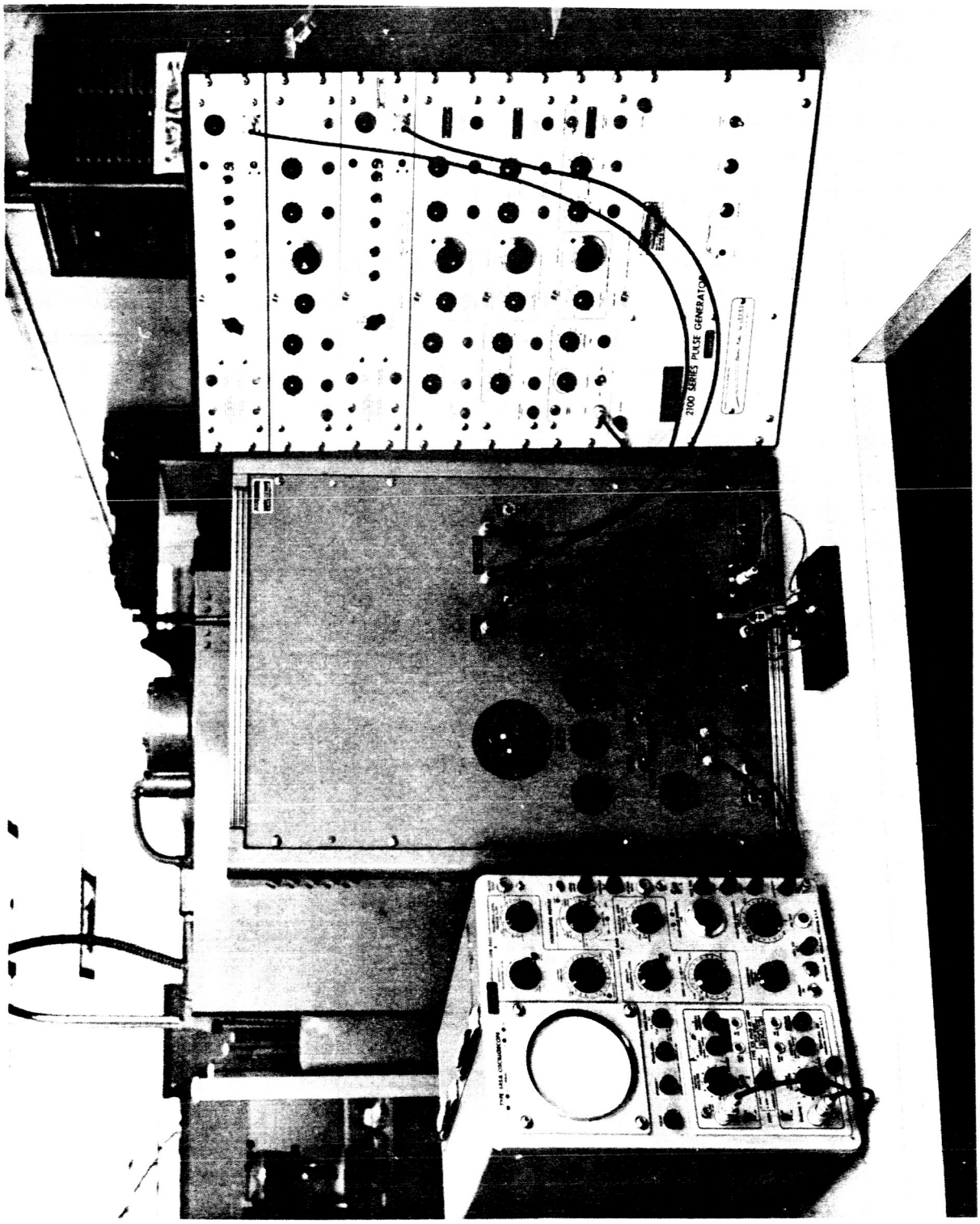


FIG. 28



COMPLETED DEVICE

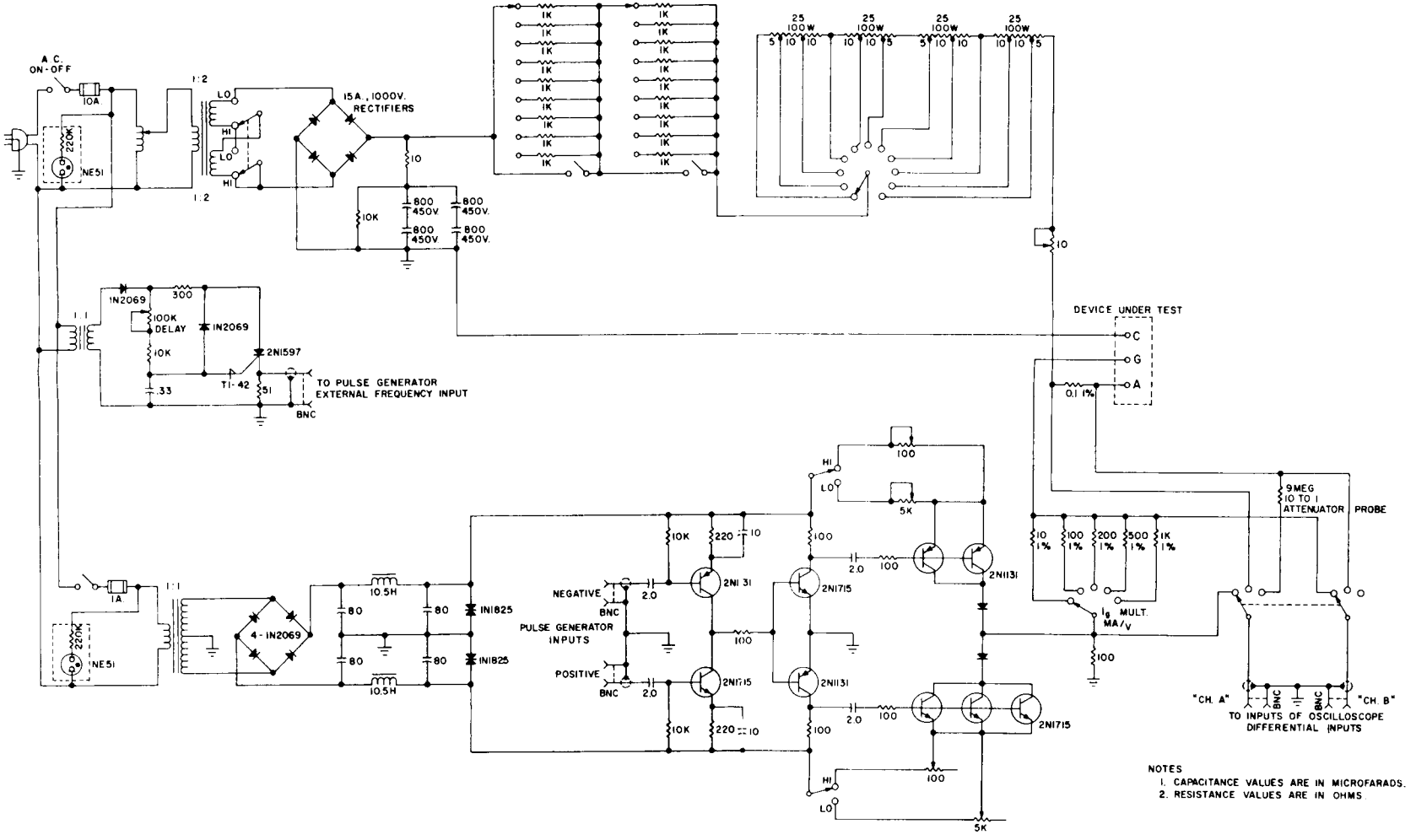
FIG. 29



POWER SWITCHING TEST SET

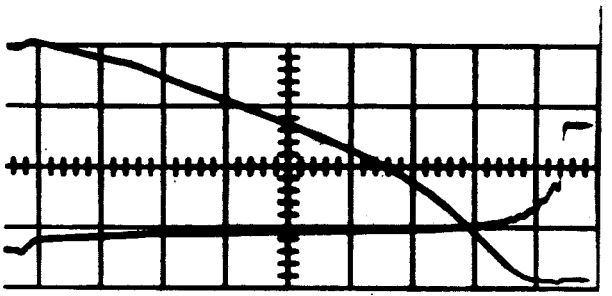
FIG. 30

G.C.S. POWER SWITCHING TEST SET



NOTES
1. CAPACITANCE VALUES ARE IN MICROFARADS.
2. RESISTANCE VALUES ARE IN OHMS.

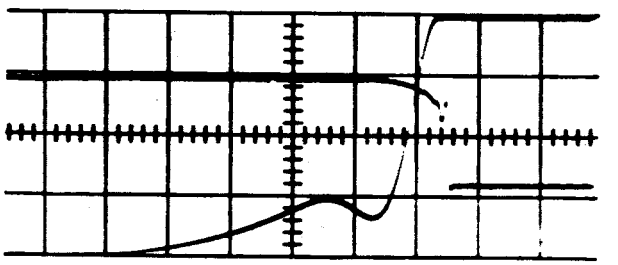
FIG. 31



G.C.S. TURN-OFF TIME

FIG. 33

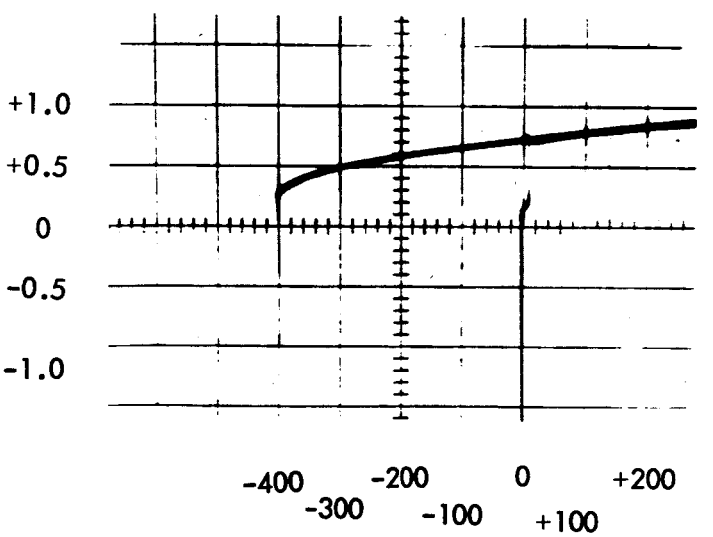
Anode Voltage = 400 v
Anode Current = 10 a
Horizontal Scale = 0.5 μs/Div.



G.C.S. TURN-ON TIME

FIG. 32

Anode Voltage = 400 v
Anode Current = 10 a
Horizontal Scale = 0.5 μs/Div.



Gate Current - ma

G.C.S. DYNAMIC GATE

CHARACTERISTIC

FIG. 34

Anode Voltage = 50 v
Anode Current = 10 a

TURN-OFF GAIN TEST SET

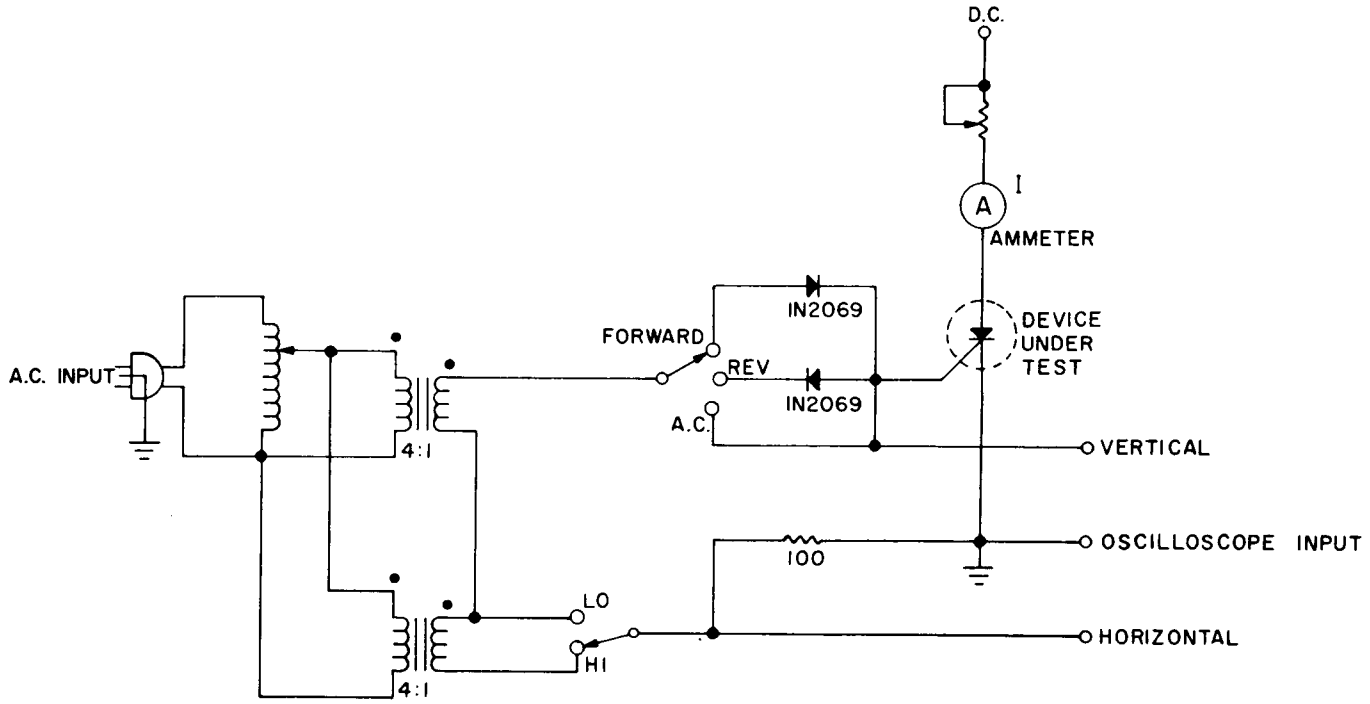
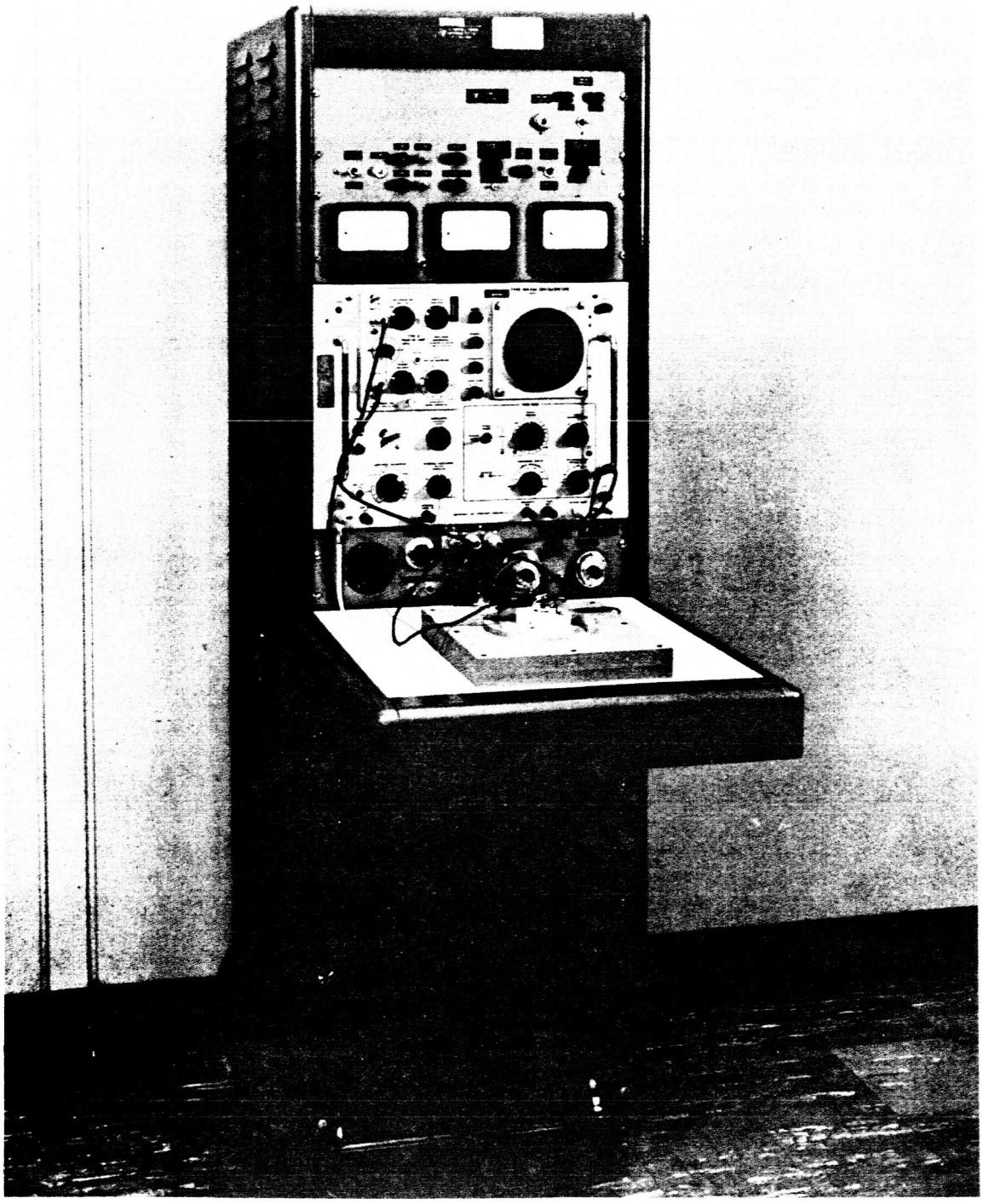
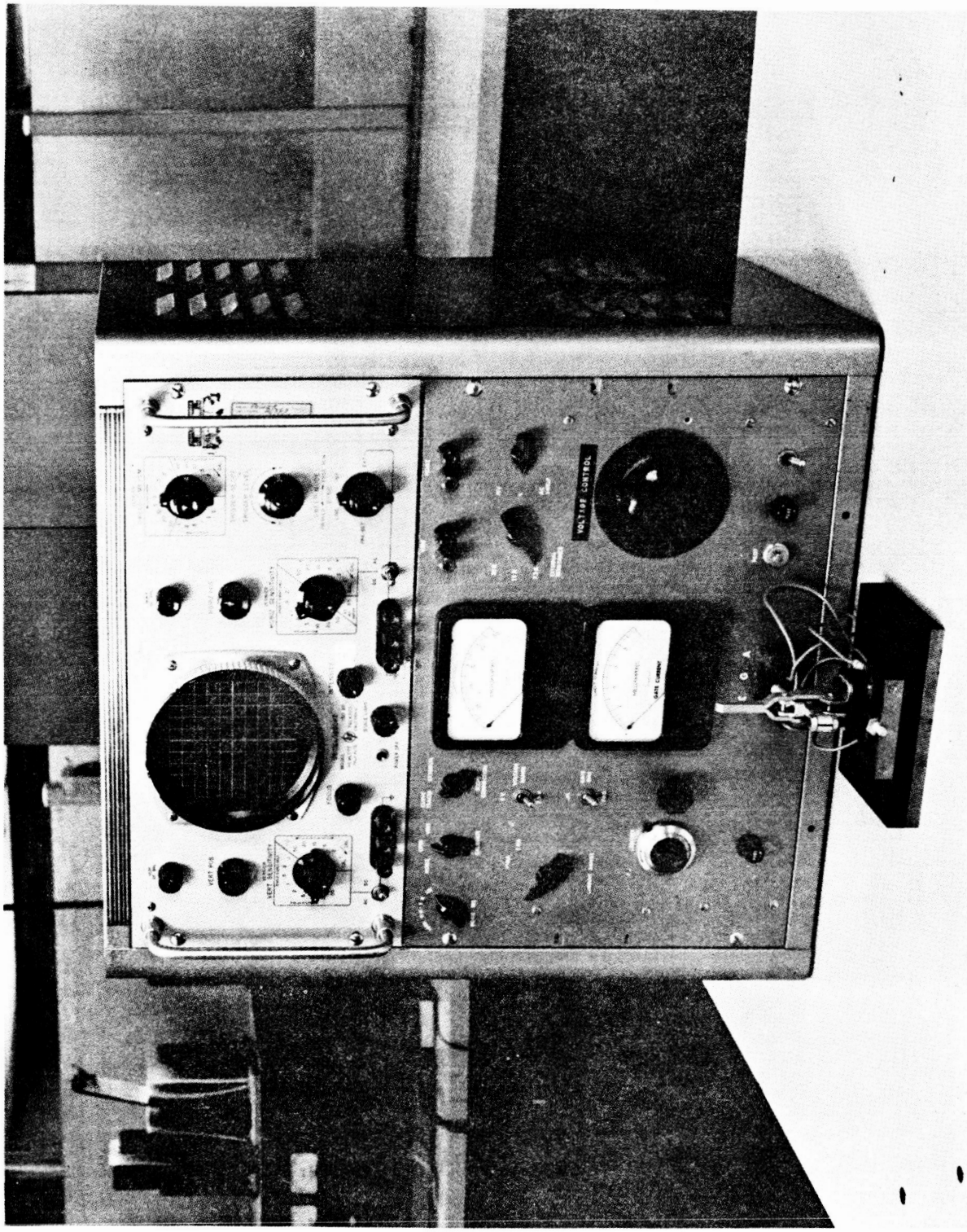


FIG. 35



THERMAL IMPEDANCE EQUIPMENT

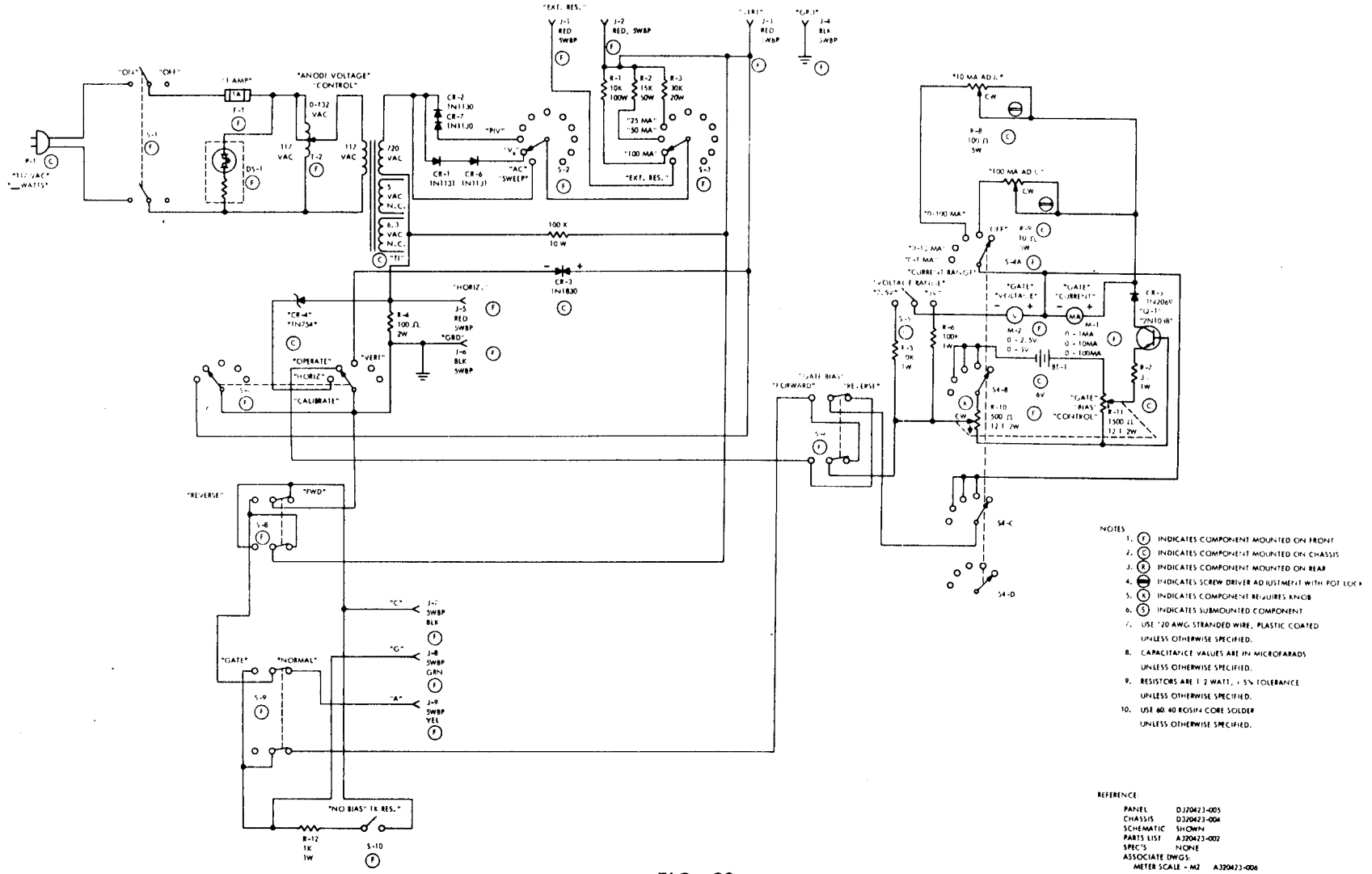
FIG. 36



PNPN CURVE TRACER TEST SET

FIG. 37

PNPN CURVE TRACER TEST SET



NOTES

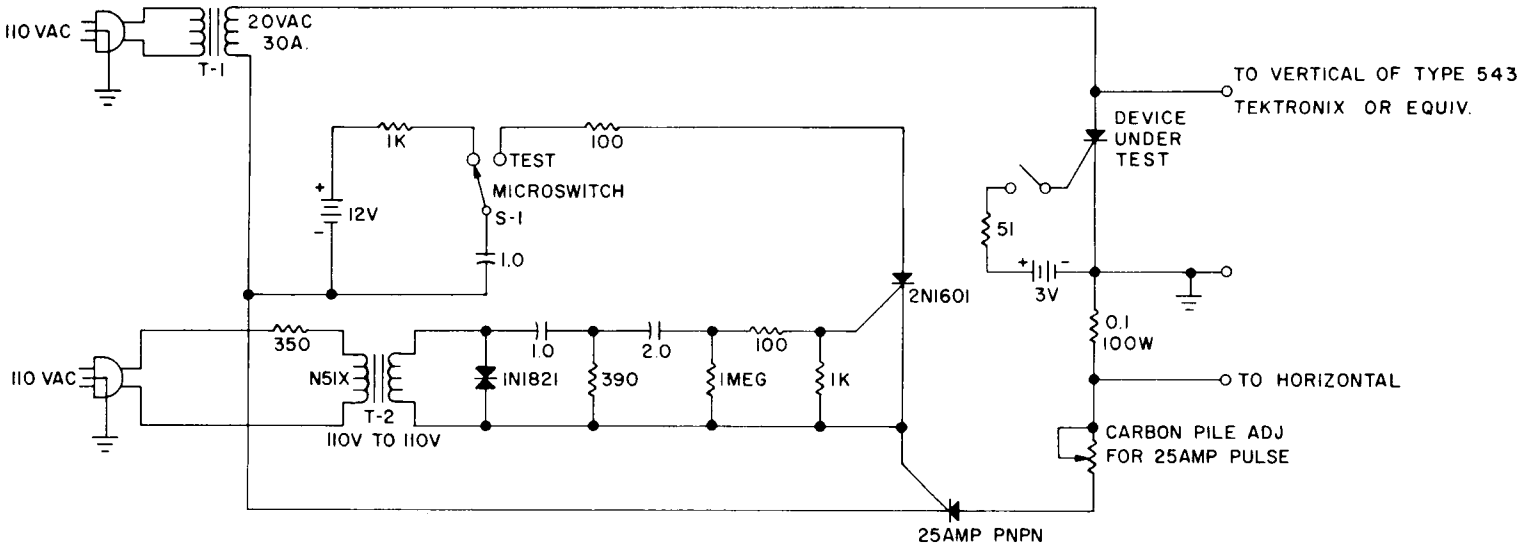
1. (F) INDICATES COMPONENT MOUNTED ON FRONT
2. (C) INDICATES COMPONENT MOUNTED ON CHASSIS
3. (R) INDICATES COMPONENT MOUNTED ON REAR
4. INDICATES SCREW DRIVER ADJUSTMENT WITH POT LOCK
5. (K) INDICATES COMPONENT REQUIRES KNOB
6. (S) INDICATES SUBMOUNTED COMPONENT
7. USE 20 AWG STRANDED WIRE, PLASTIC COATED UNLESS OTHERWISE SPECIFIED.
8. CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
9. RESISTORS ARE 1/2 WATT, ± 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.
10. USE 60/40 ROSIN CORE SOLDER UNLESS OTHERWISE SPECIFIED.

REFERENCE:

PANEL	D320423-005
CHASSIS	D320423-004
SCHEMATIC	SHOWN
PARTS LIST	A320423-002
SPEC'S	NONE
ASSOCIATE DWGS:	
METER SCALE - M2	A320423-006

FIG. 38

ANODE SURGE TEST SET



TO TEST UNIT, ACTUATE MICROSWITCH TO TEST POSITION.
CURRENT PULSE WILL BE DISPLAYED ON OSCILLOSCOPE.
MEASURE DEVICE CHARACTERISTICS BEFORE AND
AFTER PASSING CURRENT PULSE.

NOTE
1. T-1 AND T-2 SECONDARIES MUST BE IN PHASE.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. RESISTANCE VALUES ARE IN OHMS.

FIG. 39

TI-2808 DATA SHEET (16-25) FIG. 40

TAKEN BY	DATE	PAGE OF
	2/27/63	1 | 2

NASA GCS DEVICES

400 VOLT — 10 Amp

RUN No.	UNIT No.	B_{vf} (volts)	B_{vr} (volts)	I_{gs} (ma.)	I_h (ma.)	V_{gr} @10ma (volts)	V_{gf} @25ma (volts)	V_t @10 ± (volts)	$V_{gt(off)}$ @10 AMP	$I_{gt(off)}$ @10 AMP	t_d (μs) 400 volt 10 Amp	t_{on} (μs) 400 volt 10 Amp	t_s (μs) 400 volt 10 Amp	t_{off} (μs) 400 volt 10 Amp	
N31	19	460	700	11.0	130	12.0	.70	2.0	+.60	400	.07	3.2	.46	5.5	
N31	42	470	820	16.0	130	14.0	.80	1.8	+.50	300	.07	3.5	.46	3.9	
N31	59	530	920	16.0	150	13.0	.80	1.5	+.30	320	.06	3.0	.60	5.2	
N31	73	480	800	8.0	45	12.5	.80	1.3	+.20	360	.01	3.0	.54	5.6	
N31	77	480	700	16.0	125	14.0	.80	1.1	+.60	510	.07	3.0	.54	5.2	
N31	111	450	620	20.0	150	14.0	.80	2.5	+.40	240	.06	2.6	.30	4.2	
N31	113	500	840	16.0	150	13.0	.70	1.3	+.70	390	.08	3.6	.50	4.8	
N31	122	430	620	18.0	90	13.0	.90	1.4	-.60	280	.07	2.7	.80	7.2	
N31	133	480	800	6.8	25	13.0	.90	1.1	-.40	580	.06	2.3	1.80	8.0	
N31	165	440	620	16.0	75	12.0	.80	1.3	+.40	200	.05	2.5	.62	4.6	
N31	167	490	880	17.0	200	14.0	.90	1.6	+.70	380	.10	3.6	.50	5.2	
N31	173	440	700	12.0	80	13.0	.80	1.8	0.0	360	.07	3.2	.60	7.0	
N31	175	510	600	13.0	60	13.0	.80	1.2	-.30	360	.06	.40	.90	5.8	
N32	26	450	620	8.0	50	11.5	.70	1.2	+.30	590	.06	5.2	.90	6.4	
N32	89	450	600	12.0	58	13.0	.70	1.2	+.70	300	.07	5.2	.60	4.6	
N32	104	450	620	5.7	30	13.0	.80	1.3	-.10	480	.07	3.0	1.20	9.8	
N32	150	420	560	6.0	25	13.0	.70	1.4	-.10	560	.06	4.4	.70	7.3	
N32	162	440	640	5.8	28	13.0	.70	1.1	+.20	540	.05	4.1	2.3	9.0	
N32	180	440	620	7.6	40	14.0	.80	1.3	+.20	360	.06	3.6	.60	8.0	
N32	192	540	600	6.5	28	12.0	.70	1.5	+.30	440	.06	6.0	.50	6.6	
N32	205	440	560	5.0	30	12.0	.70	1.4	-.10	500	.07	3.2	1.10	9.8	
N32	221	440	600	4.1	20	14.0	.80	1.2	+.20	640	.04	4.0	1.20	9.8	
N32	223	490	620	6.3	30	13.0	.70	1.6	+.20	640	.01	5.3	.65	9.4	
N32	226	440	620	10.0	75	14.0	.80	1.7	+.40	410	.07	3.7	.42	5.5	
N31	95	490	800	11.0	120	14.0	.80	1.3	+.60	380	.09	2.4	1.0	5.2	

DATA SHEET (16-25) FIG. 40 (Cont'd)

TAKEN BY	DATE	PAGE OF
	2/27/63	2 | 2

RUN No.	UNIT No.	B_{vf} (volts)	B_{vr} (volts)	I_{gs} (ma.)	I_h (ma.)	V_{gr} @10ma (Volts)	V_{gf} @25ma (Volts)	V_f @10 Amp (volts)	$V_{gf(off)}$ @10 Amp	$I_{gf(off)}$ @10 Amp	t_d (μs) 400 volt 10 Amp	t_{on} (μs) 400 Volt 10 Amp	t_s (μs) 400 Volt 10 Amp	t_{off} (μs) 400 Volt 10 Amp	
N32	233	450	640	7.6	35	13.0	.80	1.1	+.20	660	.05	3.4	2.7	8.9	
N32	234	440	590	3.8	15	13.0	.80	1.3	−.50	520	.09	5.0	2.3	15.4	
N32	252	420	580	6.0	25	13.0	.70	1.8	+.30	480	.06	5.3	.56	7.0	
N32	257	410	550	9.0	40	12.0	.70	1.3	+.40	440	.06	6.2	.90	12.0	
N33	10	480	630	16.0	120	13.0	.90	1.6	−.70	200	.05	2.7	.60	7.6	
N33	26	550	680	1.5	8	10.5	.70	1.3	+.20	640	.09	3.4	1.8	10.8	
N33	49	420	940	3.2	15	10.0	.70	1.1	+.20	640	.12	4.1	2.3	12.0	
N33	74	470	850	3.3	20	10.0	.80	1.2	+.40	500	.09	3.5	1.2	8.4	
N33	76	450	620	20	160	12.0	.70	1.2	+.60	400	.08	3.5	.60	4.3	
N33	115	410	760	3.0	30	13.0	.70	1.3	+.40	420	.07	4.0	1.0	8.2	
N33	140	410	690	4.4	30	12.0	.80	1.3	+.40	340	.08	3.0	1.2	8.0	
N33	177	460	780	4.4	32	9.5	.80	1.4	+.10	600	.08	4.1	.74	7.4	
N33	182	560	840	5.3	22	9.0	.80	1.35	+.40	540	.06	4.6	.78	6.2	
N33	195	490	780	5.8	40	9.3	.70	1.5	+.70	440	.09	3.7	.70	5.7	
N30	55	460	660	14	120	12.0	.70	1.2	+.40	360	.07	2.8	.66	4.2	
N30	62	460	740	12	80	10.5	.70	1.1	+.40	480	.06	2.3	1.4	6.0	
N30	72	450	700	12	100	12.0	.70	1.2	+.20	240	.06	2.0	.74	5.0	
N29A	1	410	580	16	100	10.5	.70	1.1	+.70	420	.05	2.5	.46	4.2	
N29A	45	410	660	12	60	12.5	.90	1.1	+.60	300	.06	2.7	1.4	5.5	
N15	28	460	580	12	100	10.0	.65	1.1	+.25	540	.07	1.7	.75	5.5	